正基科技股份有限公司

SPECIFICATION

PRODUCT NAME：AP5236

REVISION： 1.0

DATE： JAN 8th, 2019

Customer APPROVED	
Company	
Representative Signature	

PREPARED	REVIEW		APPROVED	DCC ISSUE
	PM	QA		

正基科技股份有限公司

AP5236

Data Sheet

Address:
3F., No.15-1 Zhonghua Rd, Hsinchu Industrial Park, Hukou, Hsinchu,
Taiwan, 30352
Website:
http://www.ampak.com.tw

Revision

Revision	Date	Description	Revised By
1.0	2019 / 01 / 08	- Preliminary	Harry

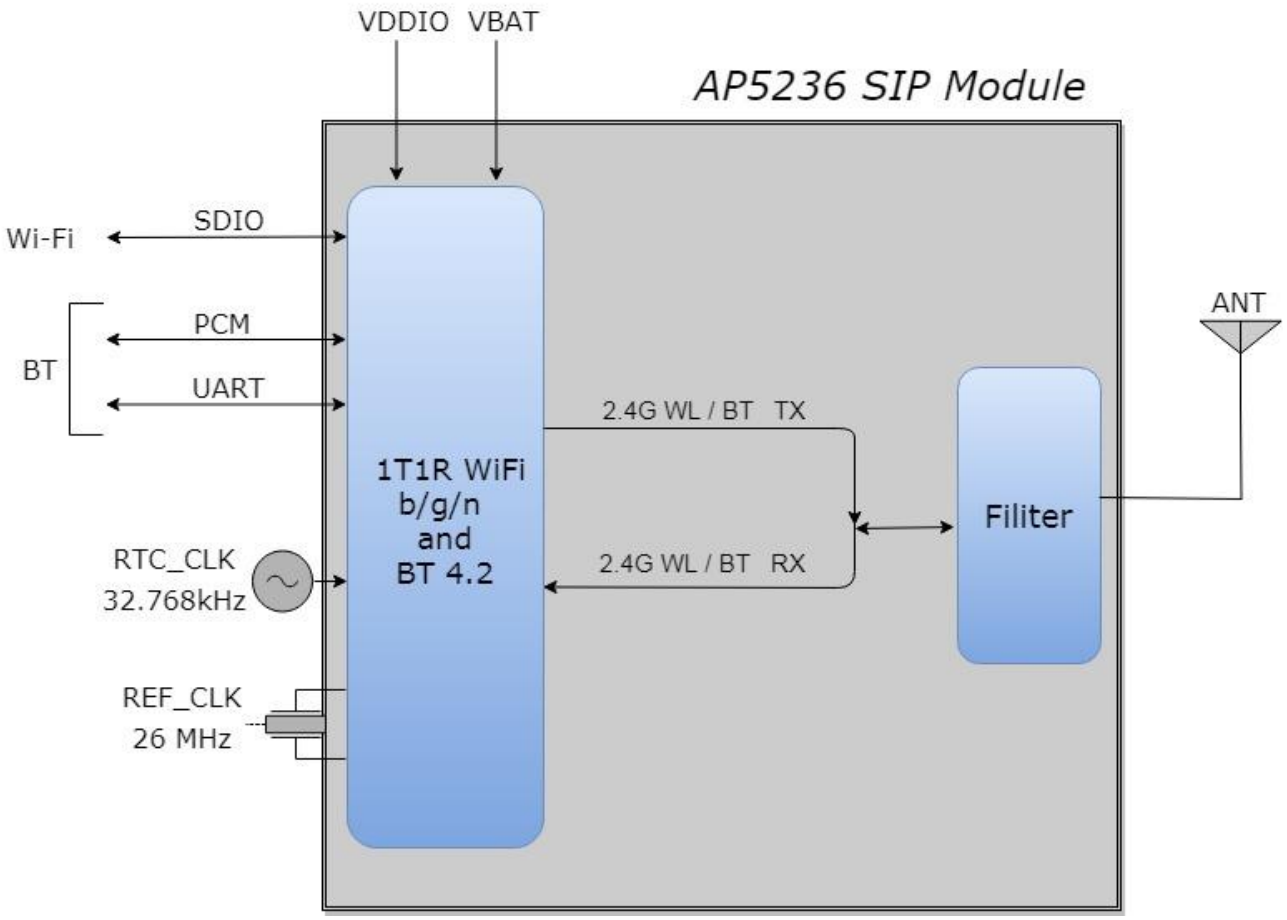
Contents

1. Introduction

1.1 Overview

AMPAK Technology would like to announce a low-cost and low-power consumption module which has all of the Wi-Fi and Bluetooth functionalities. The highly integrated module makes the possibilities of web browsing, VoIP, Bluetooth headsets and other applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11b/g/n Access Points in the wireless LAN. The wireless module complies with IEEE 802.11 b/g/n standard and it can achieve up to a speed of 72.2Mbps with single stream in 802.11n draft, 54Mbps as specified in IEEE 802.11g, or 11Mbps for IEEE 802.11b to connect to the wireless LAN. The integrated module provides SDIO interface for Wi-Fi, UART / PCM interface for Bluetooth. This compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

A simplified block diagram of the module is depicted in the figure below.



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1.2 Product Features

- 802.11b/g/n single-band radio
- Bluetooth V4.2(HS) with integrated Class 1.5 PA and Low Energy (BLE) support
- Concurrent Bluetooth, and WLAN operation
- Simultaneous BT/WLAN receive with single antenna
- WLAN host interface options:
  - SDIO v2.0 — up to 50 MHz clock rate
- BT host digital interface:
  - UART (up to 4 Mbps)
- IEEE Co-existence technologies are integrated die solution
- ECI — enhanced coexistence support, ability to coordinate BT SCO transmissions around WLAN receives

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2. General Specification

2.1 General Specification

Model Name	AP5236
Product Description	Support WiFi/Bluetooth functionalities
Dimension	L x W：6.5 x 5 (Typ.)mm、H：1.1 (Max.) mm
WiFi Interface	SDIO 2.0
BT Interface	UART / PCM
Operating temperature [a]	-30°C to 65°C
Storage temperature	-40°C to 85°C
Humidity	Operation：less than 85%
	Storage： less than 60%

Note:

a. Functionality is guaranteed across this range of temperature. Optimal RF performance as specified in the data sheet, however, is guaranteed only for –10°C to 55°C.

2.2 DC Characteristics

2.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	4.5	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	3.6	V

2.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

Voltage rails	Min.	Typ.	Max.	Unit
VBAT	3.0	3.3	3.6	V
VDDIO	1.7	3.3	3.6	V

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The module requires two power supplies: other Digital I/O Pins.

For VDDIO=1.8V	Min.	Max.	Unit
Input low voltage / Input high voltage	0.35 × VDDIO	0.65 × VDDIO	V
Output low voltage/ Output high voltage @2mA	0.45	VDDIO - 0.45	V
For VDDIO=3.3V	**Min.**	**Max.**	**Unit**
Input low voltage / Input high voltage	0.80	2	V
Output low voltage/ Output high voltage @2mA	0.4	VDDIO-0.4	V

3. Wi-Fi RF Specification

3.1 2.4GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature	Description				
WLAN Standard	IEEE 802.11b/g/n & Wi-Fi compliant				
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4GHz ISM Band)				
Number of Channels	2.4GHz：Ch1 ~ Ch13				
Modulation	802.11b : DQPSK、DBPSK、CCK 802.11 g/n : OFDM /64-QAM、16-QAM、QPSK、BPSK				
Output Power , tolerance ± 1.5 dB **The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard**					
802.11b	**1Mbps**	**2Mbps**	**5.5Mbps**	**11Mbps**	
	17	17	17	17	
802.11g	**6、9Mbps**	**12、18Mbps**	**24Mbps**	**36Mbps**	**48Mbps**
	16	16	16	16	15
	54Mbps				
	15				
802.11n 20MHz	**MCS0~2**	**MCS3**	**MCS4**	**MCS5**	**MCS6**
	17	17	16	15	14
	MCS7				
	14				
Note： The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.					

Sensitivity, tolerance ± 2 dB CCK modulation PER ≦ 8%、OFDM modulation PER ≦ 10%				
802.11b	Data Rate	Spec.(dBm)		
	1Mbps	-95		
	2Mbps	-92		
	5.5Mbps	-90		
	11Mbps	-88		
802.11g	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-89	24Mbps	-82
	9Mbps	-87	36Mbps	-79
	12Mbps	-86	48Mbps	-76
	18Mbps	-84	54Mbps	-73
802.11n_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS4	-79
	MCS1	-86	MCS4	-75
	MCS2	-84	MCS6	-73
	MCS3	-82	MCS7	-71
Maximum Input Level	802.11b : -10 dBm			
	802.11g/n : -20 dBm			

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4. Bluetooth Specification

4.1 Bluetooth Specification

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

Feature	**Description**	
General Specification		
Bluetooth Standard	Bluetooth V4.2 of 1, 2 and 3 Mbps.	
Host Interface	UART	
Frequency Band	2402 MHz ~ 2480 MHz	
Number of Channels	79 channels for classic	
Modulation	FHSS, GFSK, DPSK, DQPSK, 8DPSK	
RF Specification		
	CL1 (dBm)	**CL2** (dBm)
BDR Output Power	**6**	2
EDR Output Power	4	2
LE Output Power	5	2
	Typical.	
Sensitivity @ BER=0.1% for GFSK (1Mbps)	-86 dBm	
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)	-87 dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)	-82 dBm	
Maximum Input Level	GFSK (1Mbps):-20dBm	
	π/4-DQPSK (2Mbps) :-20dBm	
	8DPSK (3Mbps) :-20dBm	

Note*：The Bluetooth output power is able to be configured by firmware (hcd file).

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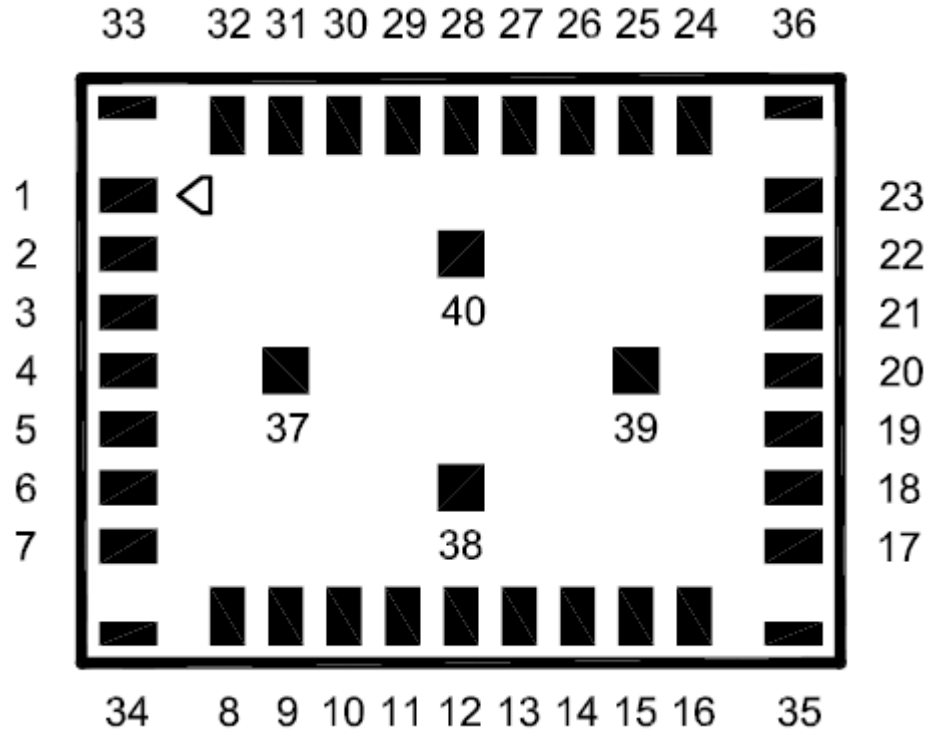
5. Pin Definition

5.1 Pin Outline

< TOP VIEW >



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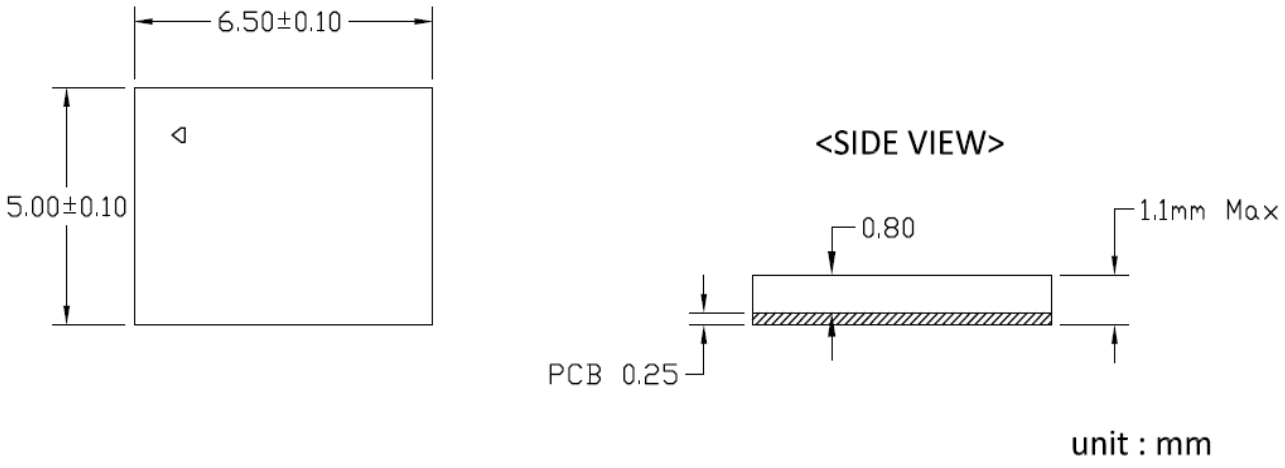
5.2 Pin Assignment

NO	Name	Type	Description
1	WL_BT_ANT	I/O	RF I/O port
2	GND	—	Ground connections
3	WL_REG_ON	I	WLAN device enable/disable pin
4	WL_HOST_WAKE	O	WLAN device to wake-up HOST
5	GND	—	Ground connections
6	XTAL_IN	I	Crystal input
7	XTAL_OUT	O	Crystal output
8	SDIO_DATA_CLK	I/O	SDIO clock line
9	SDIO_DATA_CMD	I/O	SDIO command line
10	SDIO_DATA_2	I/O	SDIO data line 2
11	SDIO_DATA_0	I/O	SDIO data line 0
12	SDIO_DATA_3	I/O	SDIO data line 3
13	SDIO_DATA_1	I/O	SDIO data line 1
14	LPO	I	External Low Power Clock input (32.768KHz)
15	VIN_LDO_OUT	P	Internal Buck voltage generation pin
16	VBAT	P	Main power voltage source input
17	SR_VLX	P	Internal Buck voltage generation pin
18	GND	—	Ground connections
19	VDDIO	P	I/O Voltage supply input
20	UART_TXD	O	Bluetooth UART interface
21	UART_RXD	I	Bluetooth UART interface
22	UART_CTS_N	I	Bluetooth UART interface
23	UART_RTS_N	O	Bluetooth UART interface
24	PCM_CLK	I/O	PCM clock
25	PCM_SYNC	I/O	PCM sync signal
26	PCM_OUT	O	PCM Data output
27	PCM_IN	I	PCM data input
28	BT_WAKE	I	HOST wake-up Bluetooth device
29	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
30	BT_REG_ON	I	Bluetooth device enable/disable pin
31	WL_GPIO1	I/O	WLAN GPIO
32	WL_GPIO2	I/O	WLAN GPIO

33	GND	—	Ground connections
34	GND	—	Ground connections
35	GND	—	Ground connections
36	GND	—	Ground connections
37	GND	—	Ground connections
38	GND	—	Ground connections
39	GND	—	Ground connections
40	GND	—	Ground connections

6. Dimensions

6.1 Module Dimensions



PHYSICAL DIMENSIONS

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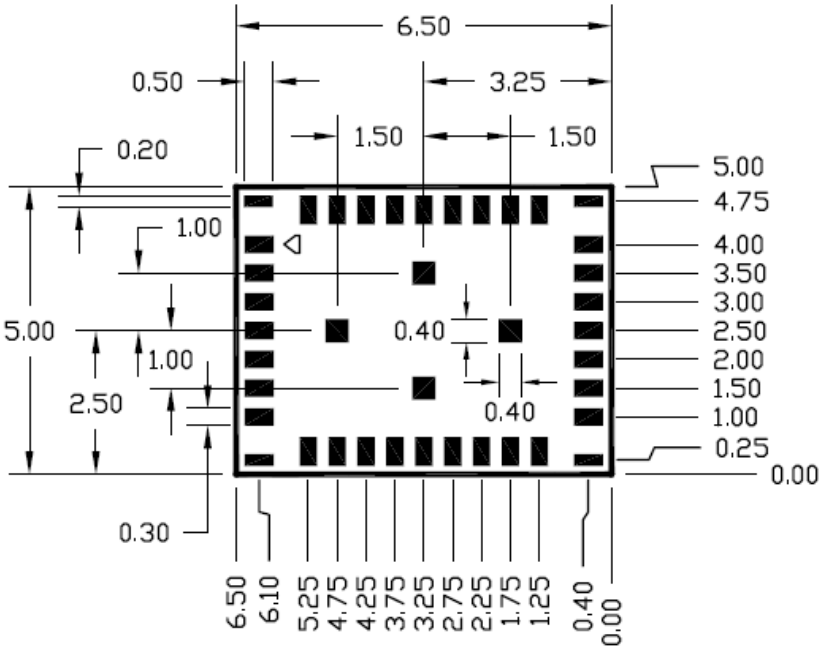
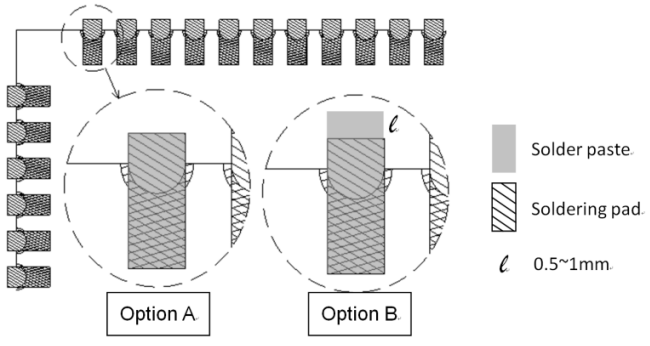
6.2 Recommended Footprint

< TOP VIEW >



unit : mm

- Solder paste layer design is generally the same as recommended footprint.
  (錫膏層設計通常建議和焊墊尺寸相同)
- If soldering quality with good wetting on upright side is essential for PQC, how to optimize the aperture design in the stencil to adjust the amount of solder paste would be crucial.
  In addition, a kind of stencil design with stepped thickness in partial area would be considered if the thickness of stencil is about 0.1mm or thinner. Please optimize the stencil design by manufacture engineer or contact AMPAK FAE for assistance.
  (如果模組吃錫品質考量側面爬錫，如何優化鋼網開孔設計以調整適當的錫膏量是非常重要的。尤其鋼網的厚度大約是 0.1mm 或更薄時，可考慮局部加厚鋼網的設計。請諮詢製程工程師以優化鋼網的設計,或是聯絡正基科技技術支持團隊).



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7. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-200	ppm
Duty cycle	30 - 70	%
Input signal amplitude	200 to 3300	mV, p-p
Signal type	Square-wave or sine wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<10000	ppm
Output high voltage	0.7Vio - Vio	V

Input signal amplitude follow VDDIO (1.8V or 3.3V)

External Ref_CLK signal characteristics

No.	Item	Symb.	Electrical Specification				Remark
			Min.	Type	Max.	Units	
1	Nominal Frequency	F0		26.00000		MHz	
2	Mode of Vibration			Fundamental			
3	Frequency Tolerance	ΔF/F0	-10	-	10	ppm	at 25℃±3℃
4	Operating Temperature Range	T_{OPR}	-30	-	85	℃	
5	Frequency Stability	TC	-10	-	10	ppm	
6	Storage Temperature	T_{STG}	-55	-	125	℃	
7	Load capacitance	CL	-	16		pF	
8	Equivalent Series Resistance	ESR	-	-	50	Ω	
9	Drive Level	DL	-	100	200	μW	
10	Insulation Resistance	IR	500	-	-	MΩ	At 100V_{DC}
11	Shunt Capacitance	C0	-	-	3	pF	
12	Aging Per Year	Fa	-2	-	2	ppm	First Year

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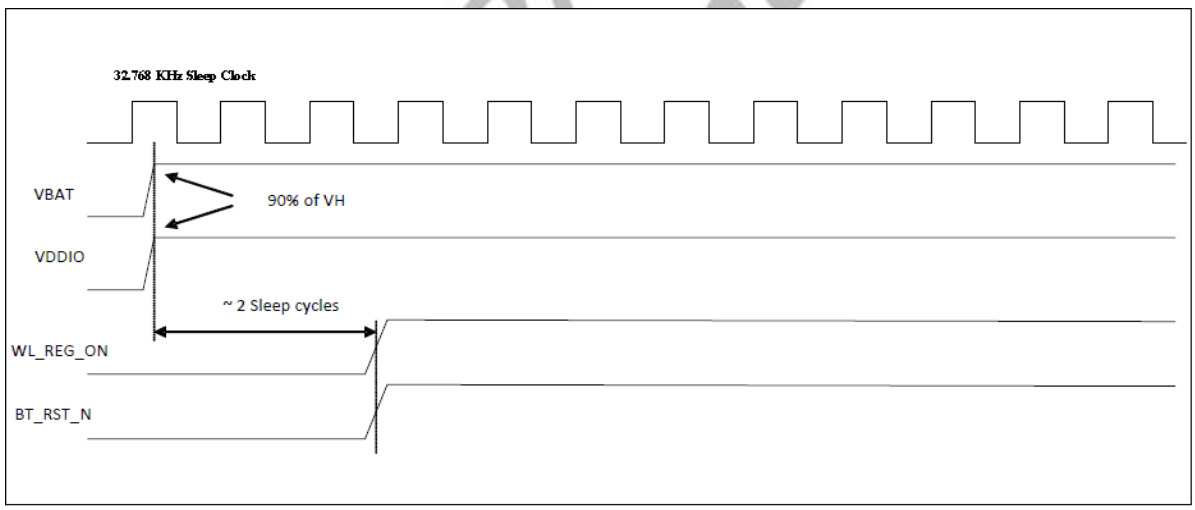
8. Host Interface Timing Diagram

8.1 Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.
Additionally, diagrams are provided to indicate proper sequencing of the signals for carious operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

※ WL_REG_ON: Used by the PMU to power up the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.

※ BT_RST_N: Low asserting reset for Bluetooth only. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



WLAN=ON, Bluetooth=ON

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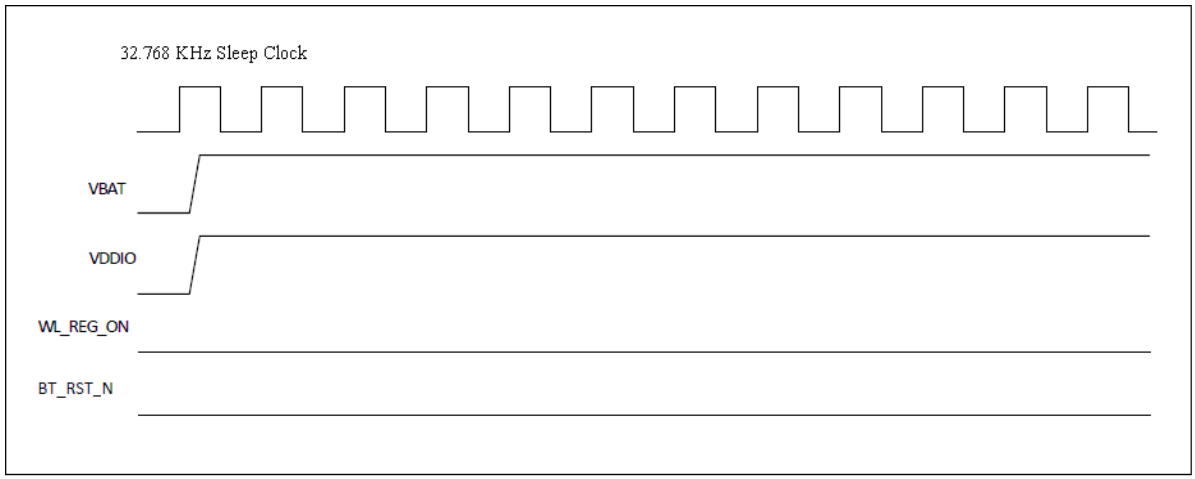
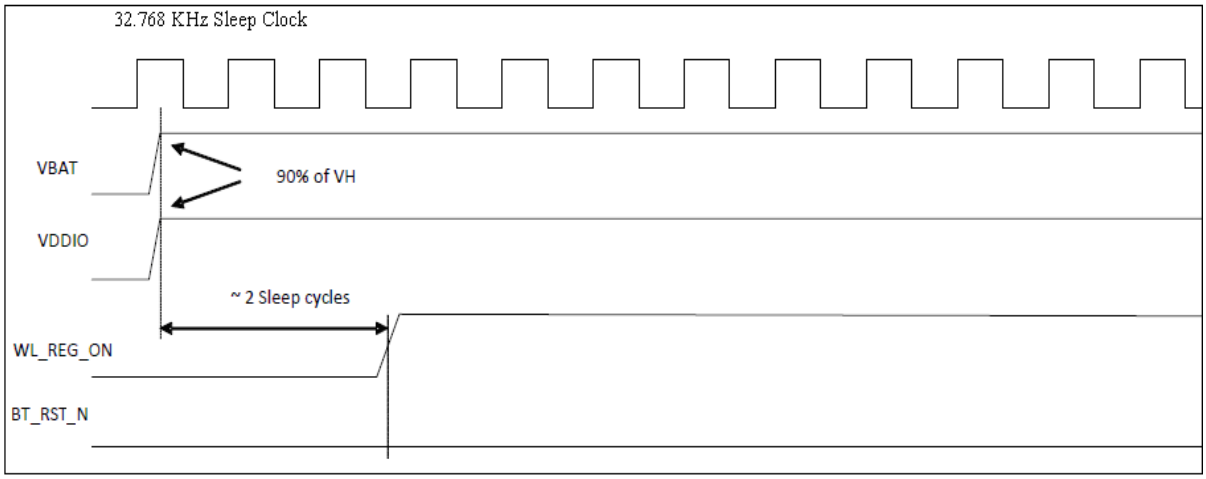
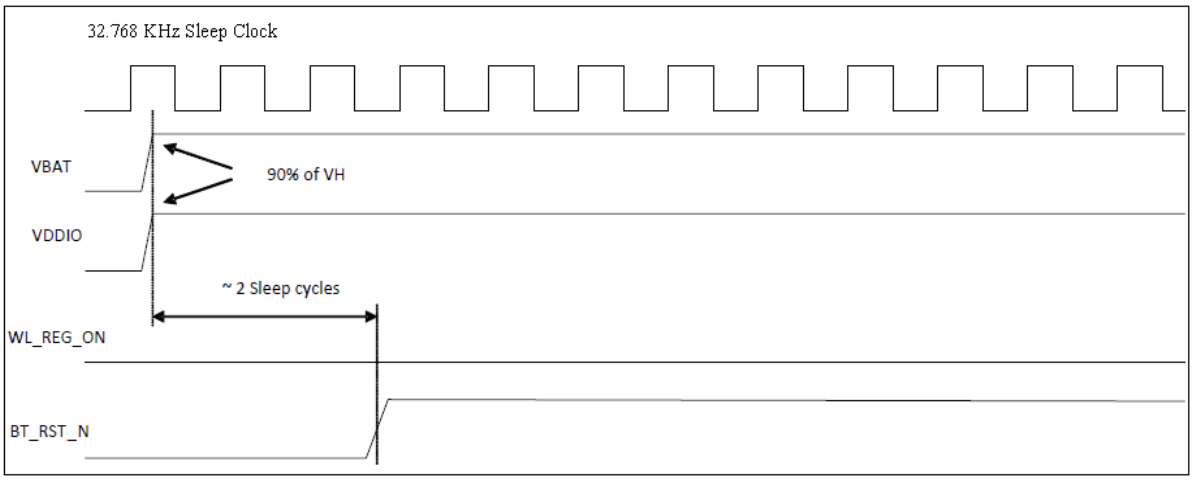


WLAN=OFF, Bluetooth=OFF



WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

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8.2 SDIO Pin Description

The module supports SDIO version 2.0 for 4-bit modes (100 Mbps), and high speed 4-bit (50 MHz clocks – 200 Mbps). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- Function 0 Standard SDIO function (Max Block Size / Byte Count = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max Block Size / Byte Count = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max Block Size / Byte Count = 512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

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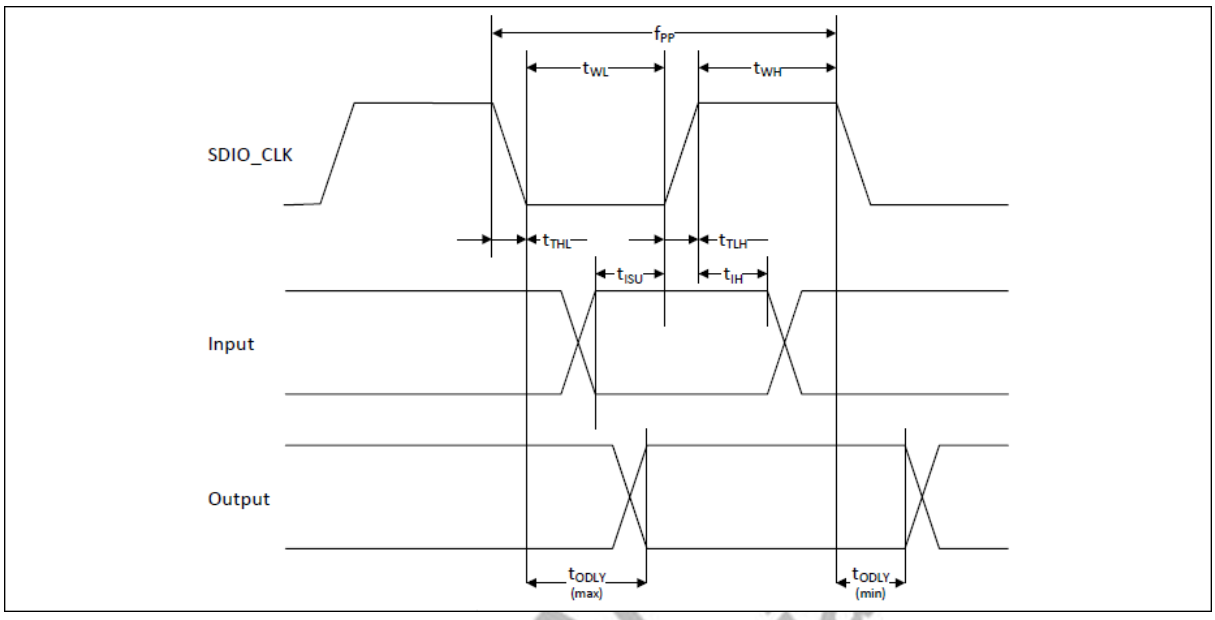
8.3 SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL[b])					
Frequency-Data Transfer mode	fPP	0	-	25	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	-	14	ns
Output delay time – Identification mode	tODLY	0	-	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

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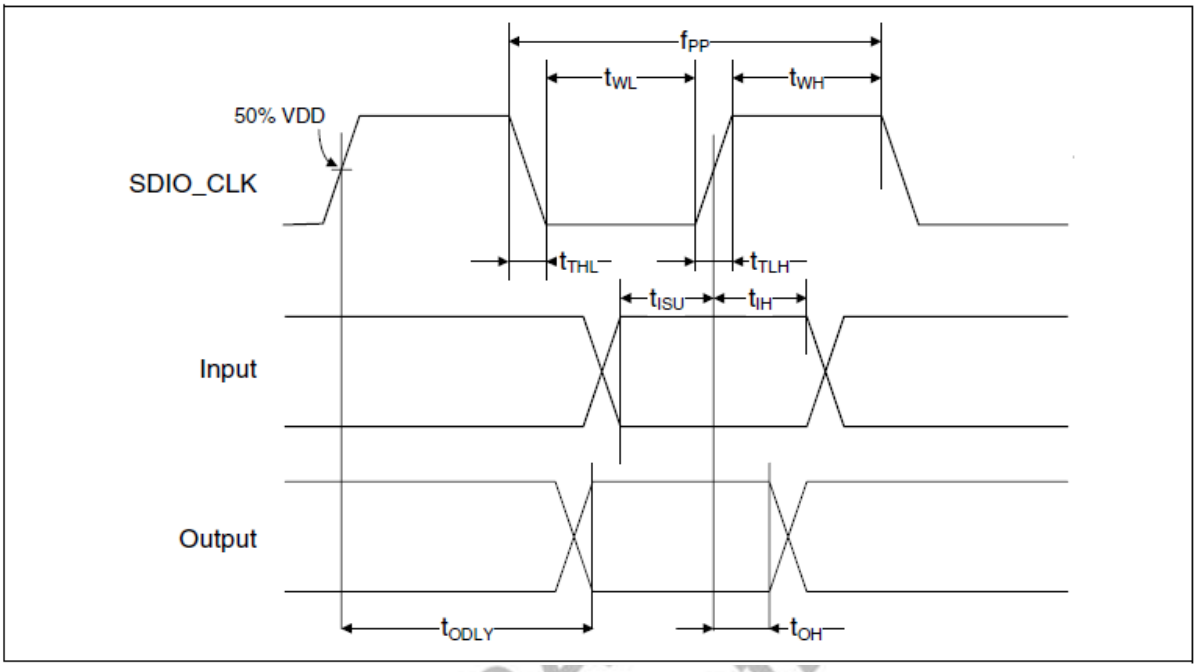
8.4 SDIO High Speed Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are refferred to minimum VIH and maximum VIL[b])					
Frequency-Data Transfer mode	fPP	0	-	50	MHz
Frequency-Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7	-	-	ns
Clock rise time	tTLH	-	-	3	ns
Clock low time	tTHL	-	-	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	6	-	-	ns
Input hold time	tIH	2	-	-	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	-	-	14	ns
Output hold time	tOH	2.5	-	-	ns
Total system capacitance (each line)	CL	-	-	40	pF

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 x VDDIO and max(Vil) = 0.2 x VDDIO.

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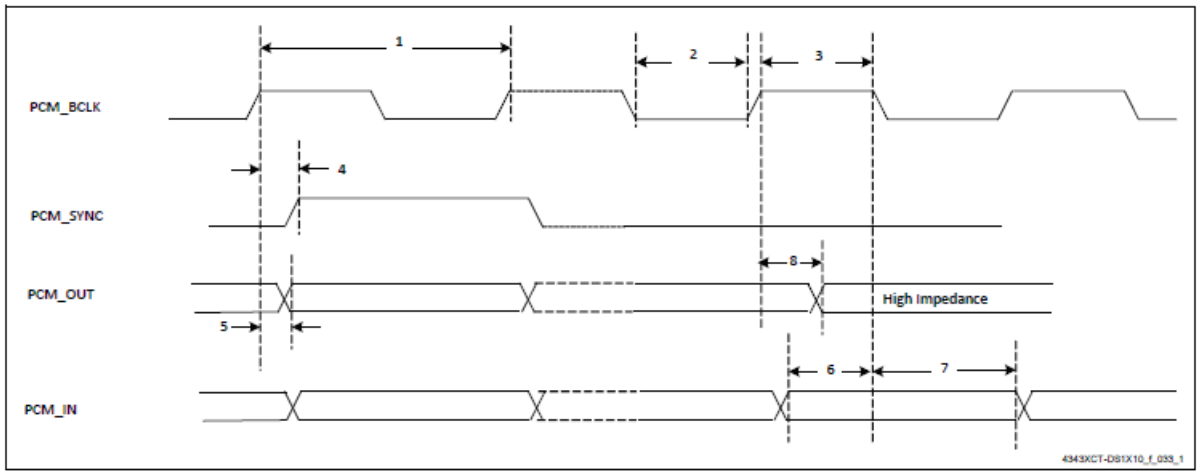
8.5 UART Interface Timing

Short Frame Sync, Master Mode

PCM Timing Diagram (Short Frame Sync, Master Mode)

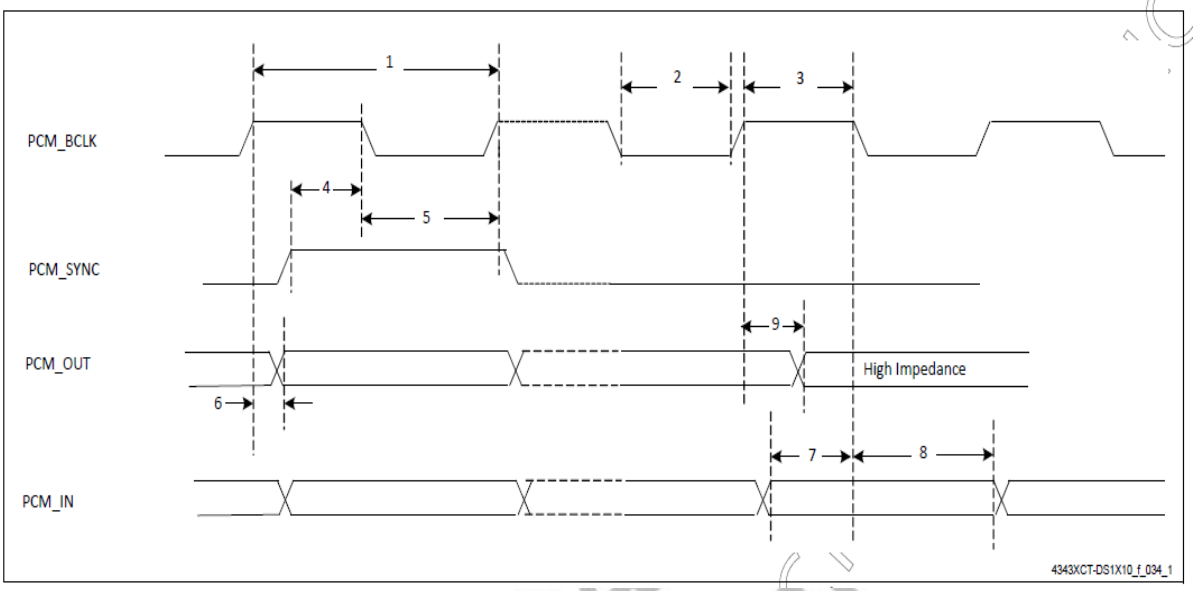


PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Slave Mode

PCM Timing Diagram (Short Frame Sync, Slave Mode)



PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

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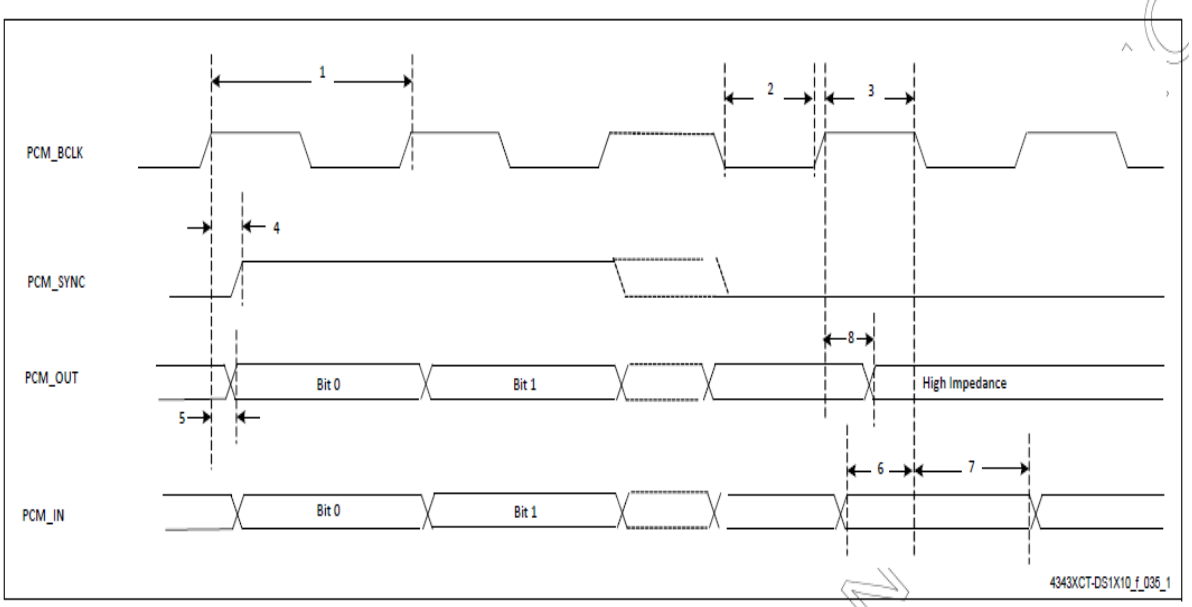
Long Frame Sync, Master Mode

PCM Timing Diagram (Long Frame Sync, Master Mode)

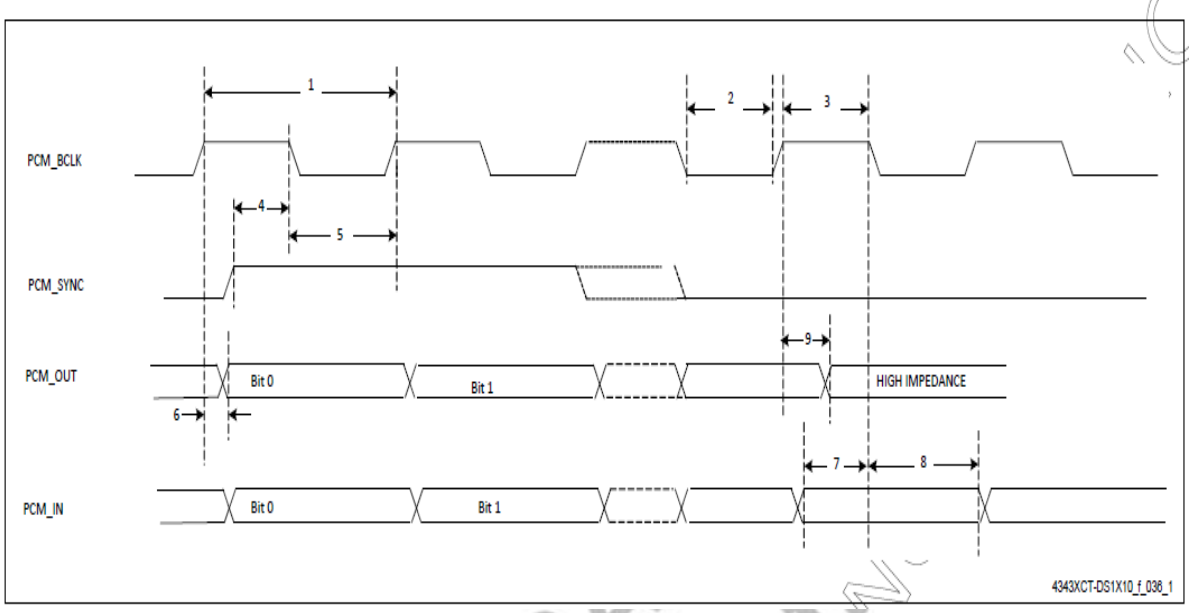


PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Slave Mode

PCM Timing Diagram (Long Frame Sync, Slave Mode)



PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Ref No.	*Characteristics*	*Minimum*	*Typical*	*Maximum*	*Unit*
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

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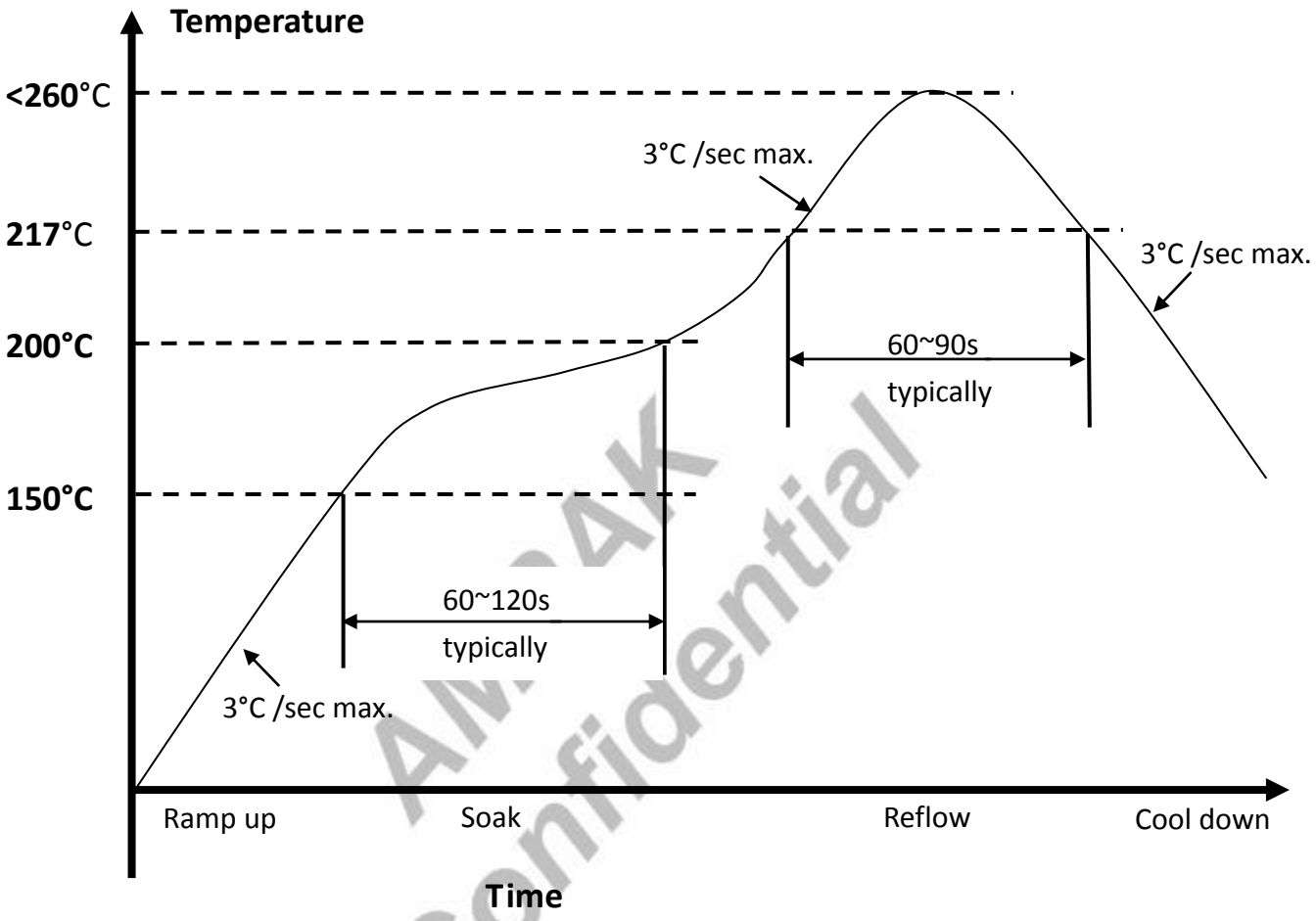
9. Recommended Reflow Profile



1. Referred to IPC/JEDEC standard
2. Peak Temperature : <260°C
3. Cycle of Reflow : 2 times max.
4. Adding Nitrogen (N2) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
5. If the shelf time is exceeded, be sure baking step to remove the moisture from the component.

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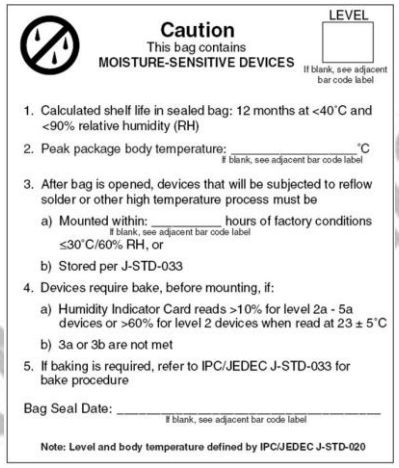
10. Package Information

10.1 Label

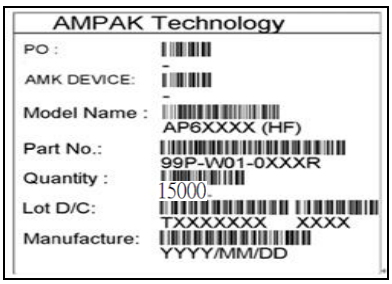
Label A→ Anti-static and humidity notice

Label B→ MSL caution / Storage Condition

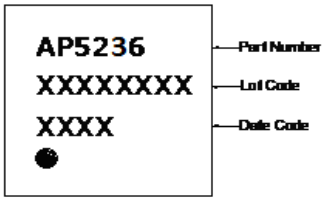


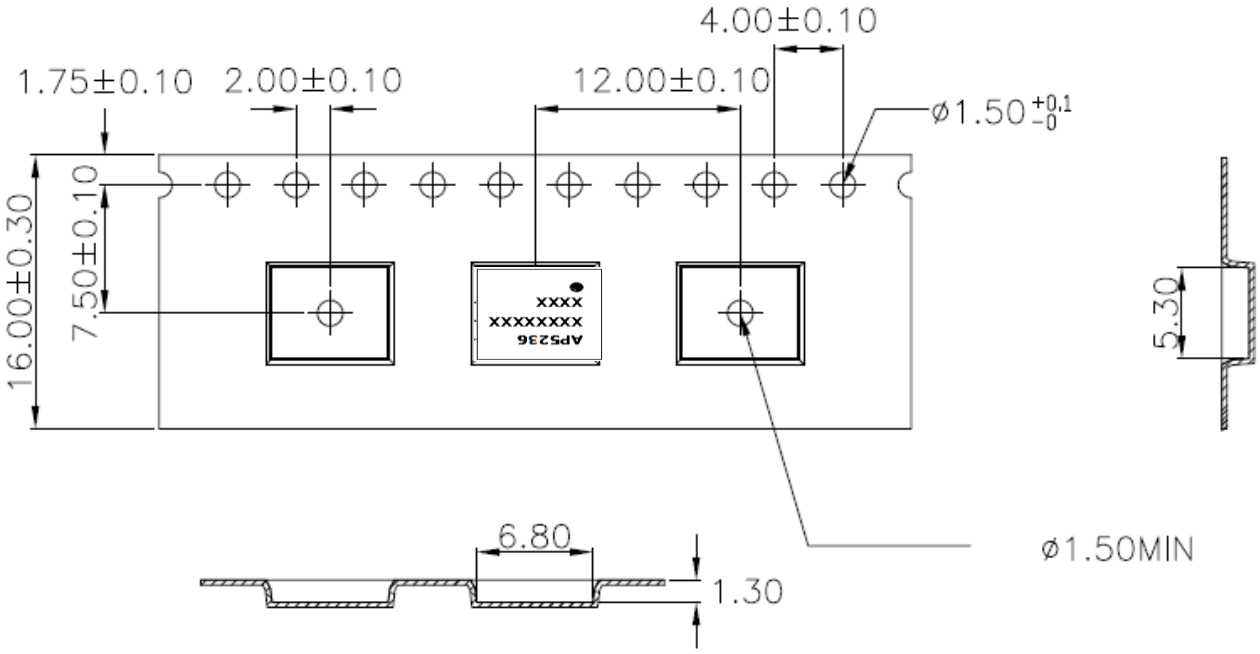
Label C→ Inner box label .

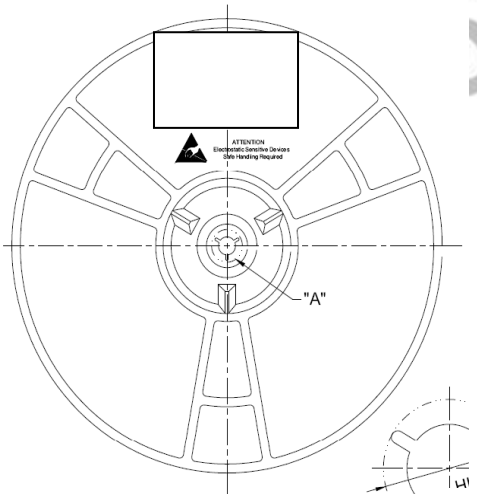
Label D→ Carton box label .

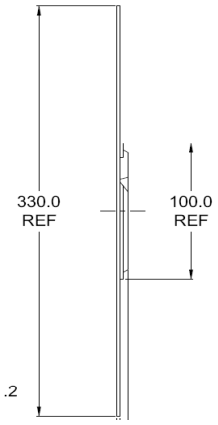


10.2 Dimension









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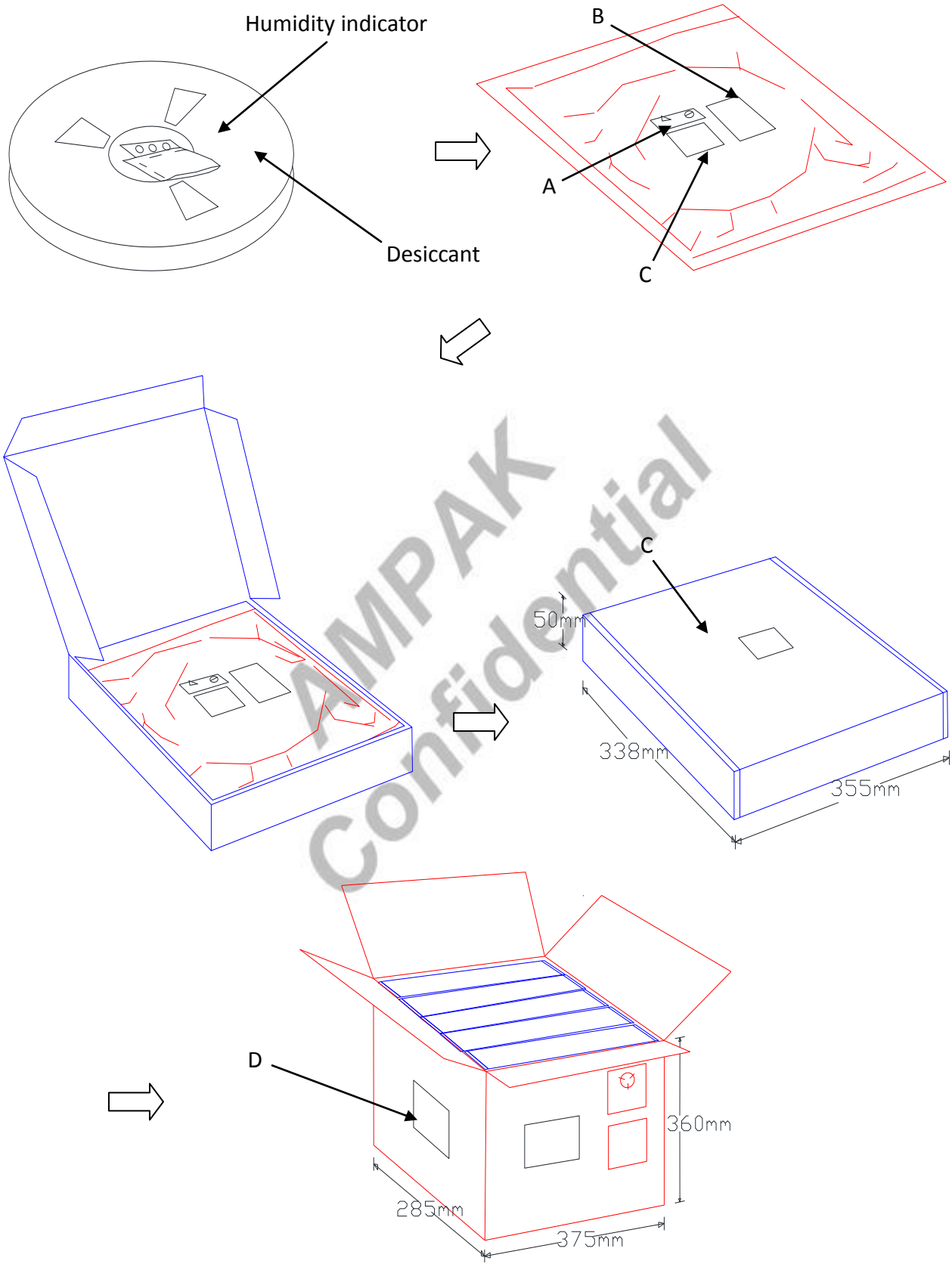
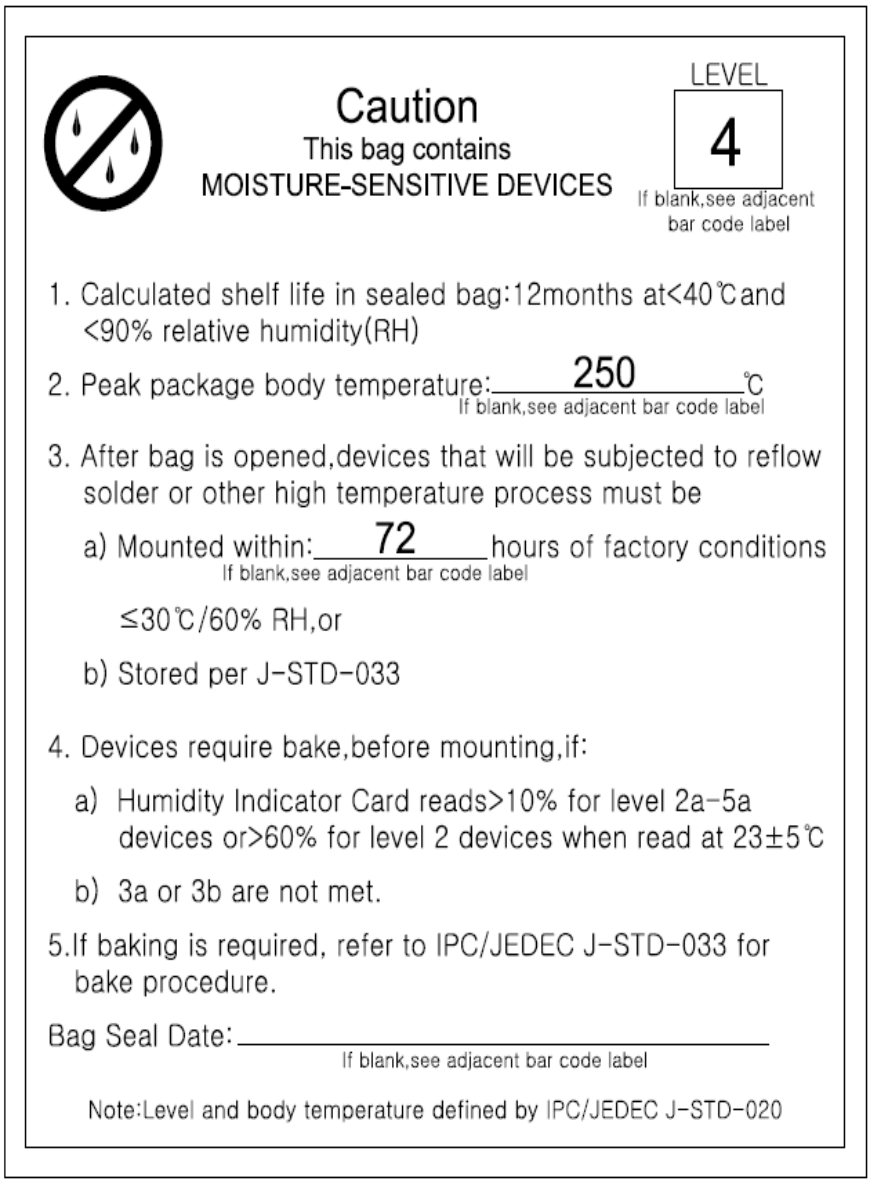


10.3 MSL Level / Storage Condition



Caution
This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL
4
If blank,see adjacent bar code label

1. Calculated shelf life in sealed bag:12months at<40℃and <90% relative humidity(RH)
2. Peak package body temperature:250℃
   If blank,see adjacent bar code label
3. After bag is opened,devices that will be subjected to reflow solder or other high temperature process must be
   a) Mounted within:72 hours of factory conditions
      If blank,see adjacent bar code label
      ≤30℃/60% RH,or
   b) Stored per J-STD-033
4. Devices require bake,before mounting,if:
   a) Humidity Indicator Card reads>10% for level 2a-5a devices or>60% for level 2 devices when read at 23±5℃
   b) 3a or 3b are not met.
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

Bag Seal Date:_____
If blank,see adjacent bar code label

Note:Level and body temperature defined by IPC/JEDEC J-STD-020

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