AMPAK Technology Inc.

正基科技股份有限公司

SPECIFICATION

PRODUCT NAME：AP5256V

REVISION： V0.3

DATE：Jan. 31st, 2023

Customer APPROVED	
Company	
Representative Signature	

PREPARED	REVIEW			APPROVED	DCC ISSUE
	PM	QA	ET		

正基科技股份有限公司

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AP5256V

Data Sheet

Address:
8F, No.15-1 Zhonghua Road, Hsinchu Industrial Park, Hukou,
Hsinchu, Taiwan, 303035
http://www.ampak.com.tw

Revision

Revision	Date	Description	Revised By
V0.1	2021/02/18	- Preliminary	Milk
V0.2	2021/09/06	-Modify packaging information	Eason
V0.3	2023/01/31	-Modify Bluetooth specification	Richard

AMPAK Technology Inc.
8F, No.15-1 Zhonghua Road, Hsinchu Industrial Park, Hukou, Hsinchu, Taiwan, 303035
http://www.ampak.com.tw

Contents

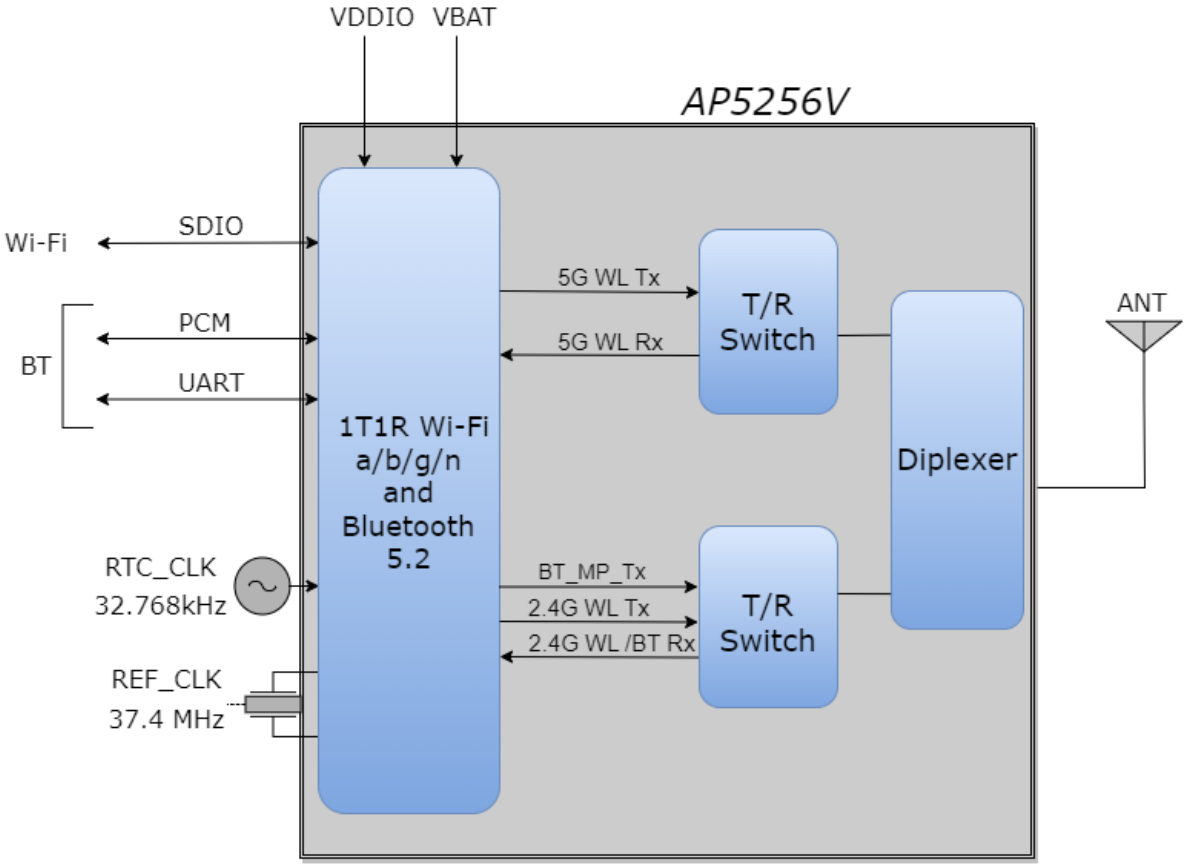
1. Introduction

1.1 Overview

AMPAK Technology would like to announce a low-cost and low-power consumption module which has all of the Wi-Fi, Bluetooth functionalities. The highly integrated module makes the possibilities of web browsing, VoIP, Bluetooth headsets applications. With seamless roaming capabilities and advanced security, also could interact with different vendors' 802.11 a/b/g/n Access Points in the wireless LAN.

The wireless module complies with IEEE 802.11 a/b/g/n standard and it can achieve up to a speed of 72Mbps with single stream in 802.11n to connect to the wireless LAN. The integrated module provides SDIO interface for Wi-Fi, UART / PCM interface for Bluetooth.

This compact module is a total solution for a combination of Wi-Fi + bluetooth technologies. The module is specifically developed for Smart phones and Portable devices.



1.2 Product Features

- IEEE 802.11a/b/g/n single-band radio with virtual-simultaneous single-band operation
- Single spatial stream up to a 72 Mbps data rate
- Supports Bluetooth V5.2 with integrated PA for Class 1.5 and Low Energy (BLE).
- Concurrent Bluetooth, and WLAN operation
- Simultaneous bluetooth/WLAN receive with single antenna
- Supports standard SDIO v2.0 and SDIO v3.0(SDR50 at 80 MHz and DDR50 at 40 MHz).
- Bluetooth host digital interface: UART (up to 4 Mbps)
- IEEE Co-existence technologies are integrated die solution
- ECI — enhanced coexistence support, ability to coordinate Bluetooth SCO transmissions around WLAN receives

.

2. General Specification

2.1 General Specification

Model Name	AP5256V
Product Description	1T1R 802.11 a/ b/g/n Wi-Fi + Bluetooth 5.2 Module
Dimension	L x W : 8 x 8(typical) mm H: 1.5(Max) mm
WiFi Interface	SDIO V3.0/2.0
Bluetooth Interface	UART / PCM
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 105°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

Note: The Optimal RF performance specified in the data sheet, however, is guaranteed only for -20~75℃.

The AP5256V is functional across this range of voltages. Optimal RF performance specified in the data sheet, however, is guaranteed only for 3.2V < VBAT < 3.8V.

2.2 DC Characteristics

2.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	-0.5	5.0	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	-0.5	2.0	V

2.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO

Voltage rails	Min.	Typ.	Max.	Unit
VBAT	3.2	3.3	3.8	V

VDDIO	1.62	1.8	1.98	V

3. Wi-Fi RF Specification

3.1 2.4GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

Feature	**Description**				
WLAN Standard	IEEE 802.11b/g/n & Wi-Fi compliant				
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4GHz ISM Band)				
Number of Channels	2.4GHz：Ch1 ~ Ch13				
Modulation	802.11b : CCK 802.11 g/n : OFDM /64-QAM、16-QAM、QPSK、BPSK				
Output Power , tolerance ± 1.5 dB **The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard**					
802.11b	**1Mbps**	**2Mbps**	**5.5Mbps**	**11Mbps**	
	17	17	17	17	
802.11g	**6、9Mbps**	**12、18Mbps**	**24Mbps**	**36Mbps**	**48Mbps**
	17	17	16.5	16.5	16
	54Mbps				
	16				
802.11n 20MHz	**MCS0~2**	**MCS3**	**MCS4**	**MCS5**	**MCS6**
	17	16.5	16.5	16	15.5
	MCS7				
	15				
Note： The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.					
Sensitivity, tolerance ± 2 dB **CCK modulation PER ≦ 8%、OFDM modulation PER ≦ 10%**					
802.11b	**Data Rate**	**Spec.(dBm)**			
	1Mbps	-95			
	2Mbps	-92			
	5.5Mbps	-90			
	11Mbps	-87			
802.11g	**Data Rate**	**Spec.(dBm)**	**Data Rate**	**Spec.(dBm)**	
	6Mbps	-91	**24Mbps**	-82	

	9Mbps	-88	**36Mbps**	-79
	12Mbps	-87	**48Mbps**	-76
	18Mbps	-85	**54Mbps**	-75
802.11n_20MHz	**Data Rate**	**Spec.(dBm)**	**Data Rate**	**Spec.(dBm)**
	MCS0	-91	**MCS4**	-79
	MCS1	-88	**MCS5**	-75
	MCS2	-85	**MCS6**	-74
	MCS3	-82	**MCS7**	-73
Maximum Input Level	802.11b : -10 dBm			
	802.11g/n : -20 dBm			

3.2 5GHz RF Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

Feature	Description
WLAN Standard	IEEE 802.11a/n/ & Wi-Fi compliant
Frequency Range	5.15~5.35GHz、5.47~5.725GHz、5.725~5.85GHz (5GHz UNII Band)
Number of Channels	5.18~5.35GHz：Ch36 ~ Ch64 5.5~5.7GHz：Ch100 ~ Ch140 5.745~5.825GHz：Ch149 ~ Ch165
Modulation	802.11a : OFDM /64-QAM、16-QAM、QPSK、BPSK 802.11n : OFDM /64-QAM、16-QAM、QPSK、BPSK

Output Power , tolerance ± 2 dB

The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard

802.11a	Frequency (MHz)	6~9Mbps	12~18Mbps	24Mbps	36Mbps
	5180~5350	14.5	14.5	14.5	14
	5500~5700	14.5	14.5	14.5	14
	5745~5825	14.5	14.5	14.5	14
	Frequency (MHz)	48Mbps	54Mbps		
	5180~5350	14	14		
	5500~5700	14	14		
	5745~5825	14	14		
802.11n 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5180~5350	14.5	14.5	14.5	14
	5500~5700	14.5	14.5	14.5	14
	5745~5825	14.5	14.5	14.5	14
	Frequency (MHz)	MCS6	MCS7		
	5180~5350	14	13.5		
	5500~5700	14	13.5		
	5745~5825	14	13.5		

Note：The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 2 dB

OFDM modulation PER ≦ 10%

802.11a	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-91	24Mbps	-81
	9Mbps	-88	36Mbps	-78

	12Mbps	-87	**48Mbps**	-74
	18Mbps	-85	**54Mbps**	-73
802.11n_20MHz	**Data Rate**	**Spec.(dBm)**	**Data Rate**	**Spec.(dBm)**
	MCS0	-91	**MCS4**	-76
	MCS1	-87	**MCS5**	-74
	MCS2	-84	**MCS6**	-73
	MCS3	-81	**MCS7**	-72
Maximum Input Level	802.11a/n : -20 dBm			
	802.11ac : -30 dBm			

4. Bluetooth Specification

4.1 Bluetooth Specification

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

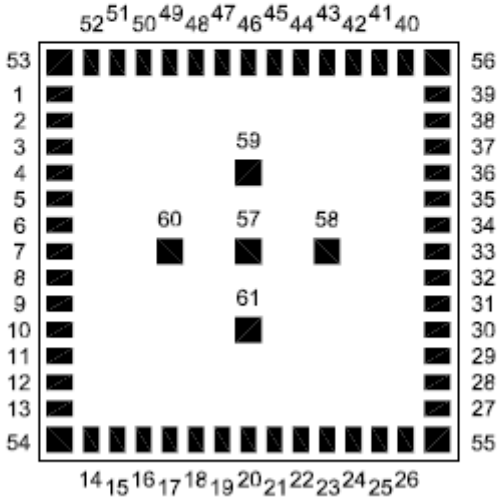
Feature	**Description**		
General Specification			
Bluetooth Standard	BDR、EDR(2、3Mbps)、LE(1、2Mbps)		
Host Interface	UART		
Frequency Band	2402 MHz ~ 2480 MHz		
Number of Channels	79 channels for classic、40 channels for BLE		
Modulation	GFSK, π/4-DQPSK, 8DPSK		
RF Specification			
	Min.	**Typical.**	Max.
BDR Output Power	6	7	11
EDR Output Power	6	7	8
BLE Output Power	7	8	9
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-86 dBm	
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)		-87 dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-83 dBm	
Sensitivity @ PER=30.8% for LE (1Mbps)		-90 dBm	
Sensitivity @ PER=30.8% for LE (2Mbps)		-88 dBm	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	π/4-DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

Note*：The Bluetooth output power is able to be configured by firmware (hcd file).

5. Pin Definition

5.1 Pin Outline

<TOP VIEW>



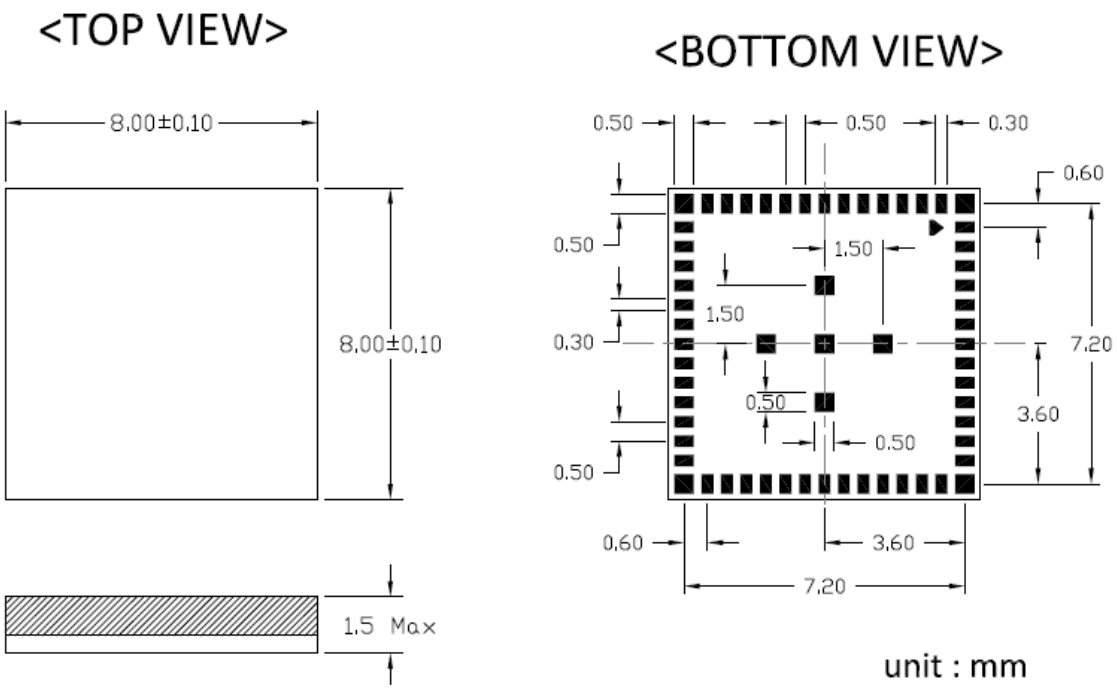
5.2 Pin Assignment

NO	Name	Type	Description
1	GND	—	Ground connections
2	GND	—	Ground connections
3	GND	—	Ground connections
4	GND	—	Ground connections
5	GND	—	Ground connections
6	GND	—	Ground connections
7	GND	—	Ground connections
8	XTAL_OP	I	Crystal input
9	XTAL_ON	O	Crystal output
10	GND	—	Ground connections
11	SDIO_DATA_CMD	I/O	SDIO command line
12	SDIO_DATA_0	I/O	SDIO data line 0
13	SDIO_DATA_1	I/O	SDIO data line 1
14	SDIO_DATA_2	I/O	SDIO data line 2
15	SDIO_DATA_CLK	I/O	SDIO clock line
16	SDIO_DATA_3	I/O	SDIO data line 3
17	GND	—	Ground connections
18	NC		Floating (Don’t connected to ground)
19	NC	—	Floating (Don’t connected to ground)
20	NC		Floating (Don’t connected to ground)
21	GND	—	Ground connections
22	VBAT	P	Main power voltage source input
23	GND	—	Ground connections
24	VDDIO	P	I/O Voltage supply input
25	GND	—	Ground connections
26	VDD_CBUCK_1P5	P	Internal CBUCK voltage input generation pin
27	SR_VLX	P	Internal CBUCK switching regulator output generation pin
28	GND	—	Ground connections
29	NC		Floating (Don’t connected to ground)
30	GND	—	Ground connections
31	LPO_IN	I	External Low Power Clock input (32.768KHz)
32	GND	—	Ground connections

33	BT_PCM_SYNC	I/O	PCM sync signal
34	BT_PCM_IN	I	PCM data input
35	BT_PCM_CLK	I/O	PCM clock
36	BT_PCM_OUT	O	PCM Data output
37	NC	—	Floating (Don't connected to ground)
38	BT_UART_RTS_N	O	Bluetooth UART interface
39	BT_UART_TXD	O	Bluetooth UART interface
40	BT_UART_RXD	I	Bluetooth UART interface
41	BT_UART_CTS_N	I	Bluetooth UART interface
42	GND	—	Ground connections
43	WL_HOST_WAKE	O	WLAN to wake-up HOST
44	WL_REG_ON	I	Power up/down internal regulators used by Wi-Fi section
45	WL_DEV_WAKE	I/O	WLAN device to wake-up HOST
46	BT_DEV_WAKE	I	HOST wake-up Bluetooth device
47	BT_HOST_WAKE	O	Bluetooth device to wake-up HOST
48	NC	—	Floating (Don't connected to ground)
49	BT_REG_ON	I	Power up/down internal regulators used by Bluetooth section
50	GND	—	Ground connections
51	WL_BT_ANT	I/O	RF I/O port
52	GND	—	Ground connections
53	GND	—	Ground connections
54	GND	—	Ground connections
55	GND	—	Ground connections
56	GND	—	Ground connections
57	GND	—	Ground connections
58	GND	—	Ground connections
59	GND	—	Ground connections
60	GND	—	Ground connections
61	GND	—	Ground connections

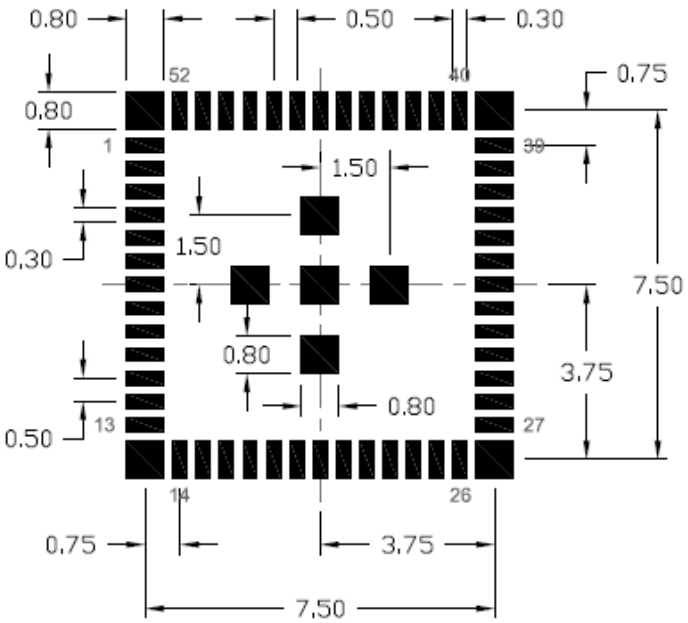
6. Dimensions

6.1 Module Dimensions

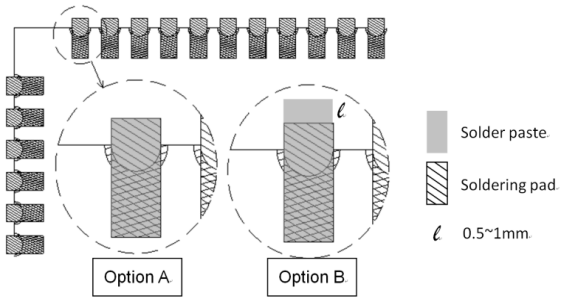


6.2 Recommended footprint

<TOP VIEW>



- Solder paste layer design is generally the same as recommended footprint.
  (錫膏層設計通常建議和焊墊尺寸相同)
- If soldering quality with good wetting on upright side is essential for PQC, how to optimize the aperture design in the stencil to adjust the amount of solder paste would be crucial.
  In addition, a kind of stencil design with stepped thickness in partial area would be considered if the thickness of stencil is about 0.1mm or thinner. Please optimize the stencil design by manufacture engineer or contact AMPAK FAE for assistance.
  (如果模組吃錫品質考量側面爬錫，如何優化鋼網開孔設計以調整適當的錫膏量是非常重要的。尤其鋼網的厚度大約是 0.1mm 或更薄時，可考慮局部加厚鋼網的設計。請諮詢製程工程師以優化鋼網的設計,或是聯絡正基科技技術支持團隊).



7. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-200	ppm
Duty cycle	30 – 70	%
Input signal amplitude	500 to 1800	mV, p-p
Signal type	Square-wave or sine-wave	-
Input impedance	>100k <5	Ω pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7Vio - Vio	V

Input signal amplitude follow VDDIO (1.8V or 3.3V)

External 37.4MHz X'TAL characteristics

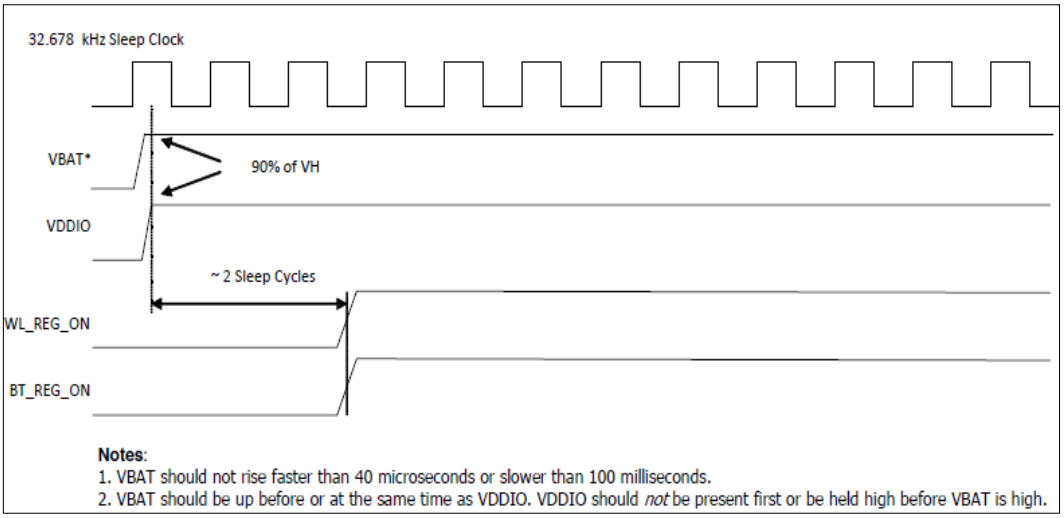
Parameter	Specification	Units
Nominal frequency - F0	37.4	MHz
Frequency Tolerance - △F / F 0 (At 25℃ +/- 3℃)	+/- 10	ppm
Operation Temperature Range - Topr	-40 ~ + 85	℃
Freq. Stability(over operating temperature) - TC Ref. to 25℃	+/- 10	ppm
Load capacitance - CL	16	pF
Equivalent Series Resistance – ESR	Max. 60	Ω
Drive Level - DL	Typ. 50, Max. 100	uW
Insulation resistance – IR At 100Vdc	Min. 500	MΩ

8. Host Interface Timing Diagram

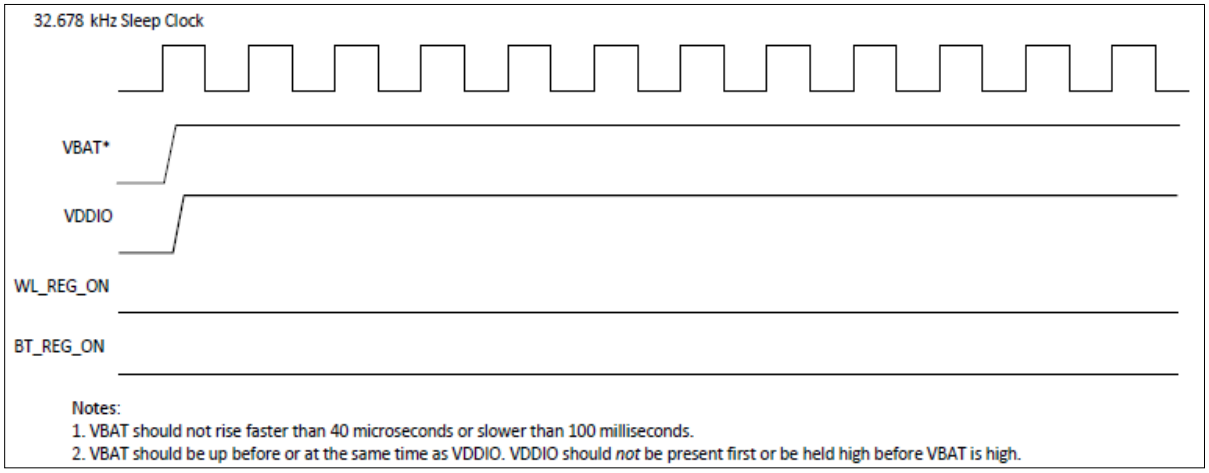
8.1 Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.
Additionally, diagrams are provided to indicate proper sequencing of the signals for carious operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

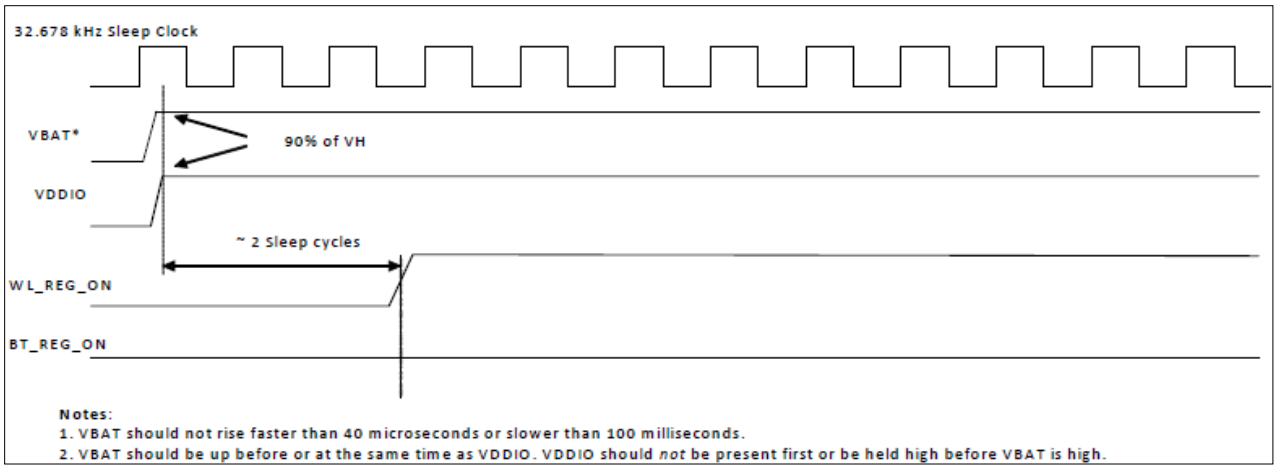
- WL_REG_ON: Used by the PMU to power up or power down the internal regulators used by the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- BT_REG_ON: Used by the PMU to power up or power down the internal regulators used by the Bluetooth section. Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



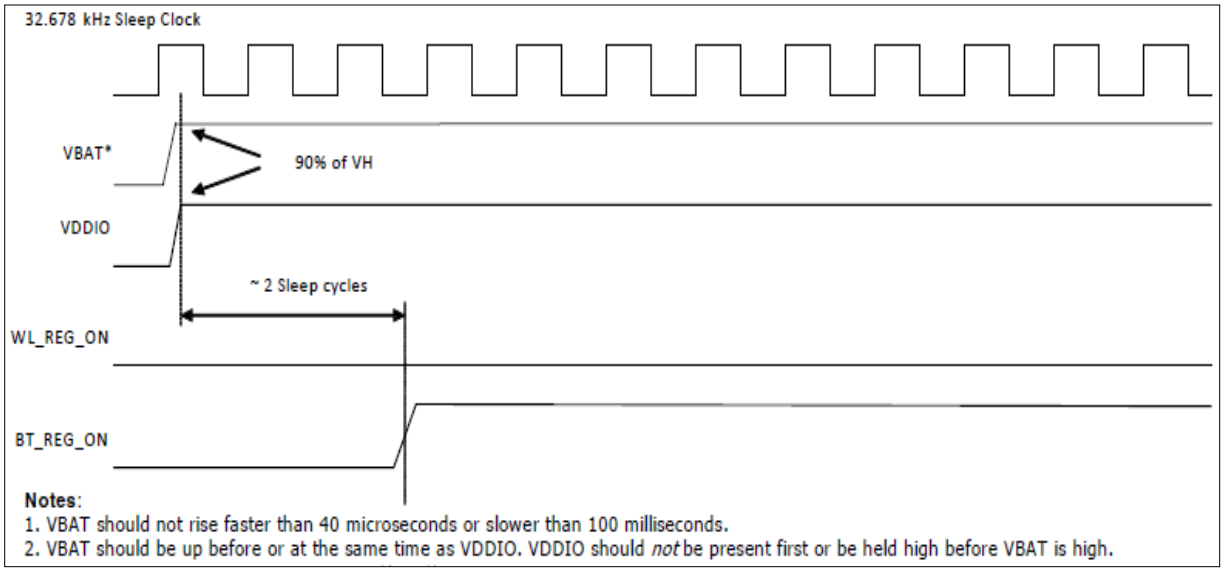
WLAN=ON, Bluetooth=ON



WLAN=OFF, Bluetooth=OFF



WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

8.2 SDIO Interface Description

The WLAN section supports SDIO version 3.0, including the new UHS-I modes:

- DS: Default speed up to 25MHz (1.8V signaling), including 1- and 4-bit modes.
- HS: High speed up to 50MH (1.8V signaling).
- SDR12: SDR up to 25MHz (1.8V signaling).
- SDR25: SDR up to 50MHz (1.8V signaling).
- SDR50: SDR up to 80MHz (1.8V signaling).
- DDR50: DDR up to 40MHz (1.8V signaling).

The SDIO interface also has the ability to map the interrupt signal onto a GPIO pin for applications requiring a different interrupt than the one provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided.

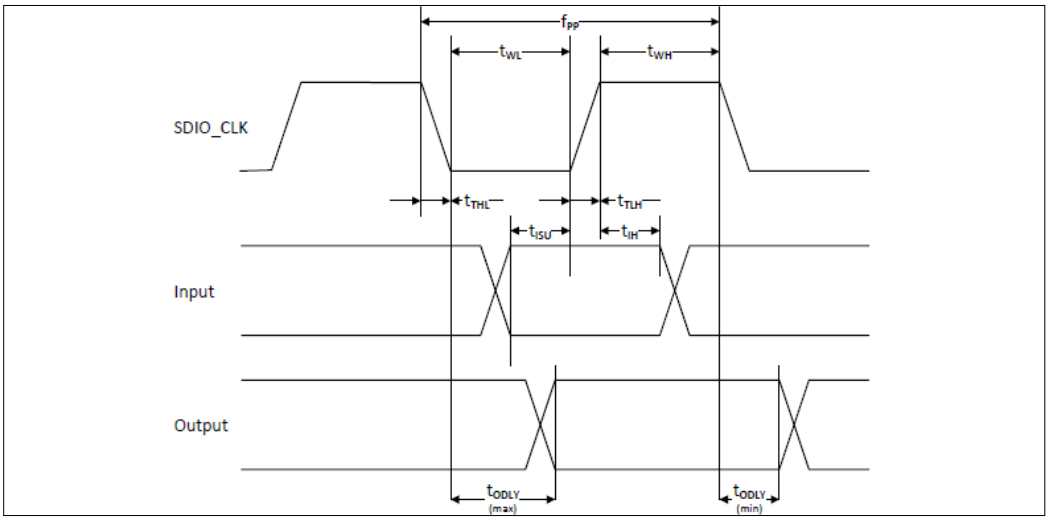
The following three functions are supported:

- Function 0 Standard SDIO function (max. BlockSize/ByteCount = 32B)
- Function 1 Backplane Function to access the internal system-on-chip (SoC) address space (max. BlockSize/ByteCount = 512B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (max. BlockSize/ByteCount = 512B).
- • Function 3 based on the SDIO Type-A Specification for Bluetooth (max. BlockSize/ByteCount = 256/256B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

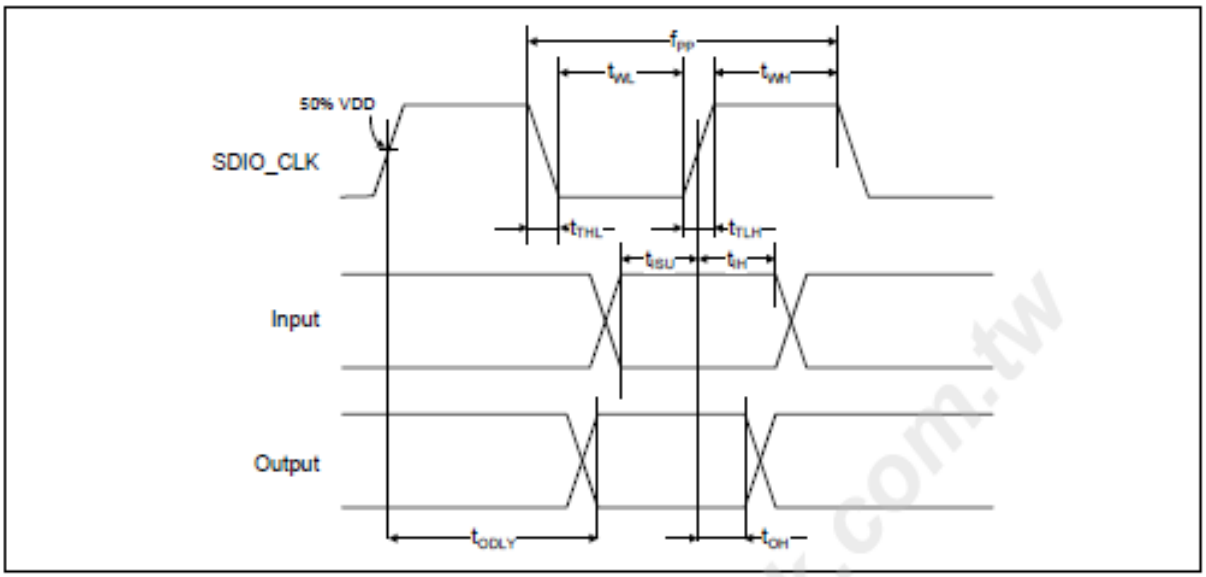
SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer mode	fPP	0	–	25	MHz
Frequency – Identification mode	fOD	0	–	400	kHz
Clock low time	tWL	10	–	–	ns
Clock high time	tWH	10	–	–	ns
Clock rise time	tTLH	–	–	10	ns
Clock low time	tTHL	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	tISU	5	–	–	ns
Input hold time	tIH	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	tODLY	0	–	14	ns
Output delay time – Identification mode	tODLY	0	–	50	ns

a. Timing is based on CL ≤ 40pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

SDIO High Speed Mode Timing Diagram

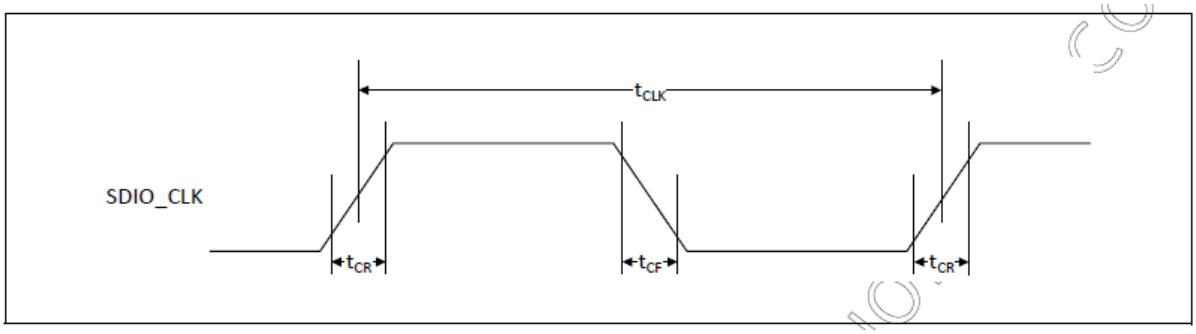


Parameter	*Symbol*	*Minimum*	*Typical*	*Maximum*	*Unit*
SDIO CLK (all values are referred to minimum VIH and maximum VIL[b])					
Frequency – Data Transfer Mode	fPP	0	–	50	MHz
Frequency – Identification Mode	fOD	0	–	400	kHz
Clock low time	tWL	7	–	–	ns
Clock high time	tWH	7	–	–	ns
Clock rise time	tTLH	–	–	3	ns
Clock low time	tTHL	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	tISU	6	–	–	ns
Input hold Time	tIH	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	tODLY	–	–	14	ns
Output hold time	tOH	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on CL ≤ 40 pF load on CMD and Data.
b. min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

SDIO Bus Timing Specifications in SDR Modes

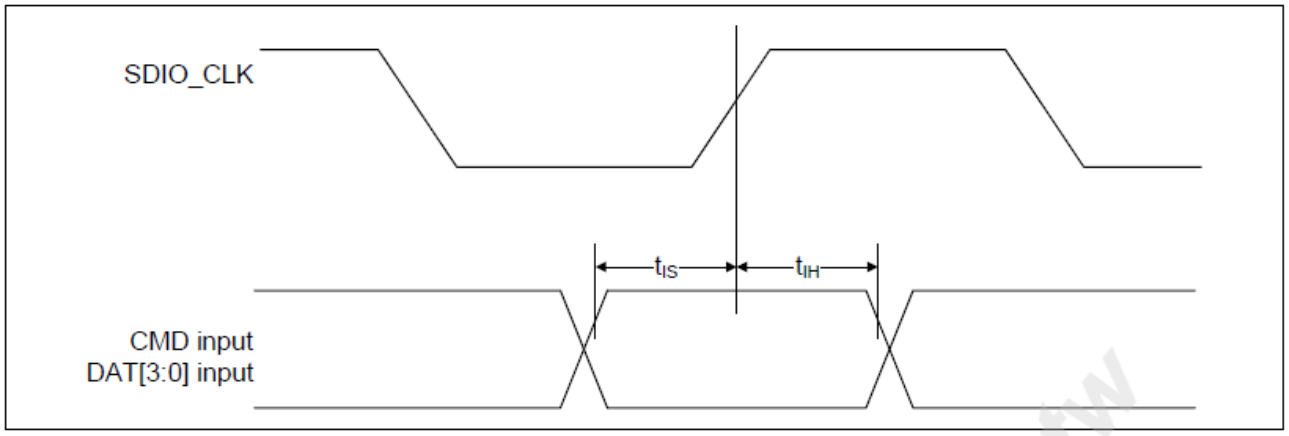
Clock timing(SDR Modes)



Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	40	–	ns	SDR12 mode
		20	–	ns	SDR25 mode
		12.5	–	ns	SDR50 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max) @ 100 MHz, C_{CARD} = 10 pF t_{CR}, t_{CF} < 0.96 ns (max) @ 208 MHz, C_{CARD} = 10 pF
Clock duty cycle	–	30	70	%	–

Card Input timing (SDR Modes)

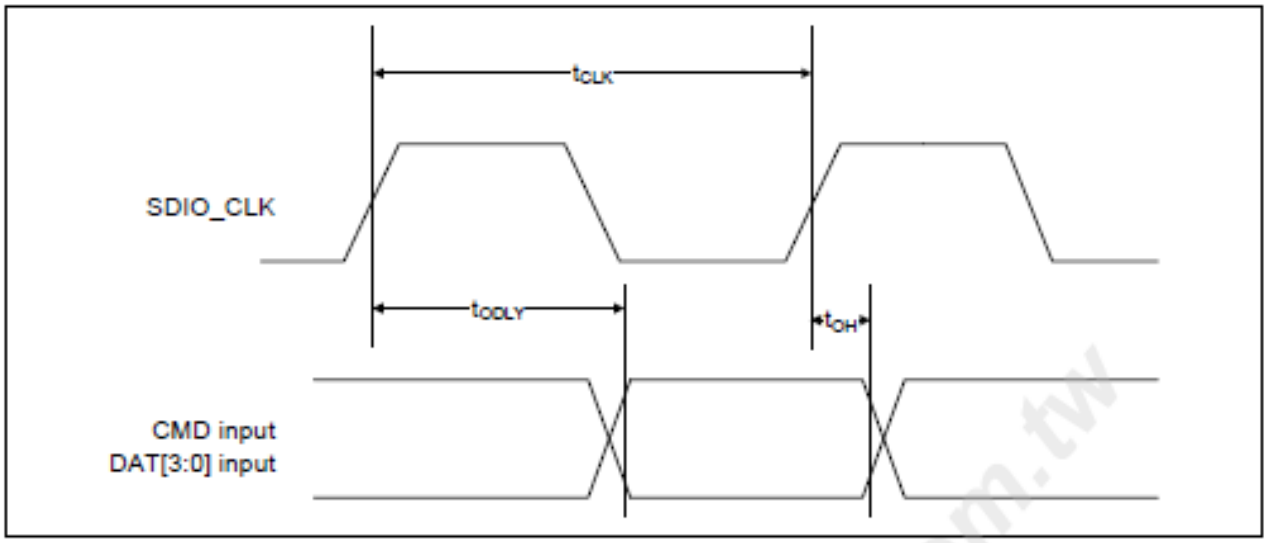
SDIO Bus Input Timing (SDR Modes)



SDIO Bus Input Timing Parameters (SDR Modes)

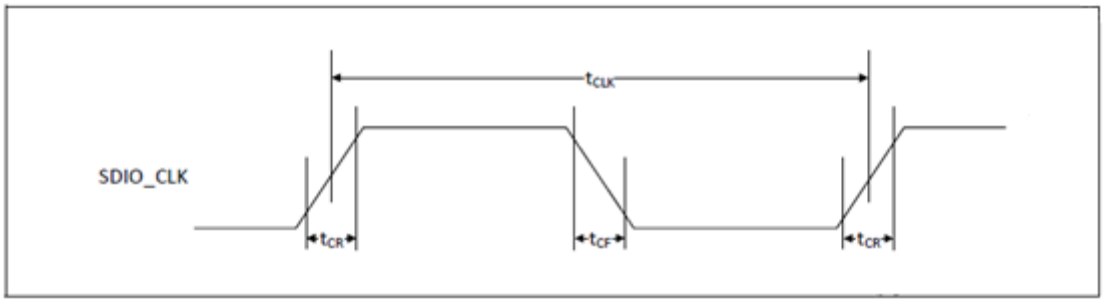
Symbol	Minimum	Maximum	Unit	Comments
SDR50 Mode				
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975V
t_{IH}	0.8	–	ns	C_{CARD} = 5 pF, VCT = 0.975V

Card output timing (SDR Modes up to 80MHz)



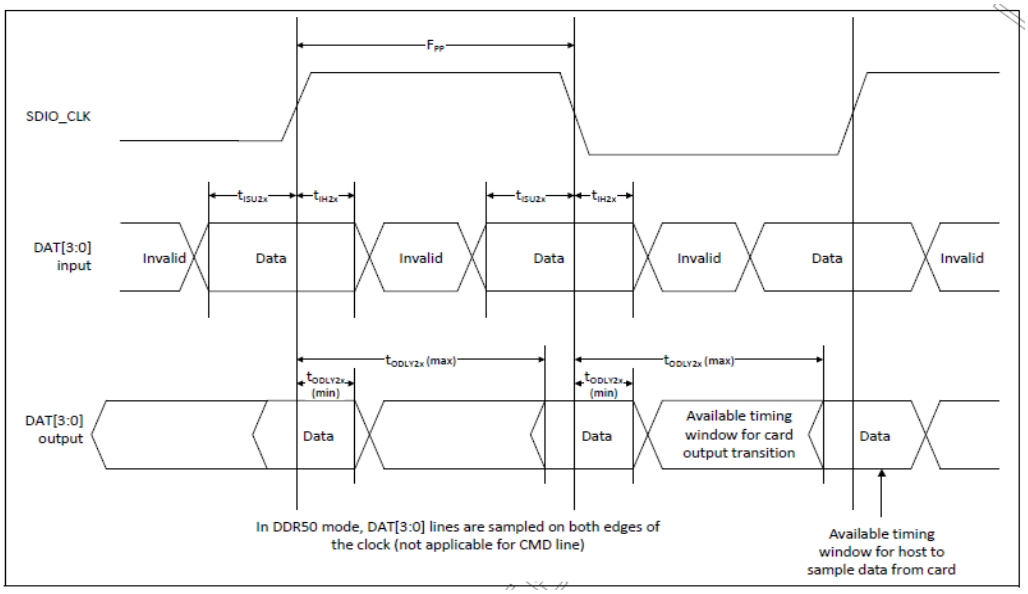
Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.5	ns	$t_{CLK} \geq 10$ ns $C_L = 30$ pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	$t_{CLK} \geq 20$ ns $C_L = 40$ pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) $C_L = 15$ pF

SDIO Bus Timing Specifications in DDR50 Mode



Parameter	Symbol	Minimum	Maximum	Unit	Comments
–	t_{CLK}	25	–	ns	DDR50 mode
–	t_{CR},t_{CF}	–	0.2 × tCLK	ns	t_{CR}, t_{CF} < 4.00 ns (max) @50 MHz, C_{CARD} = 10 pF
Clock duty cycle	–	45	55	%	–

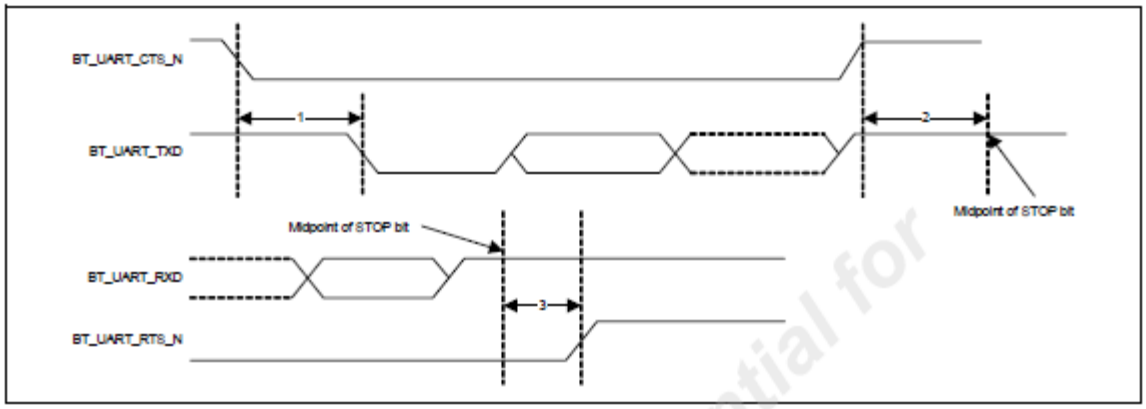
Data Timing



Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH}	0.8	–	ns	C_{CARD} < 10 pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	–	13.7	ns	C_{CARD} < 30 pF (1 Card)
Output hold time	t_{OH}	1.5	–	ns	C_{CARD} < 15 pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH2x}	0.8	–	ns	C_{CARD} < 10 pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	–	7.5	ns	C_{CARD} < 25 pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	–	ns	C_{CARD} < 15 pF (1 Card)

8.3 UART Timing

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates 115200 bps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.



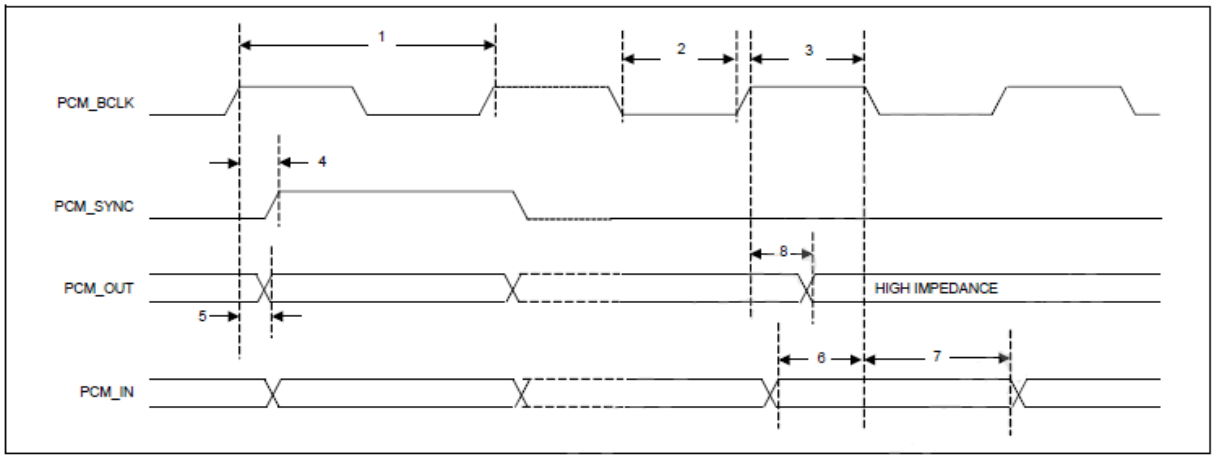
Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	—	—	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	—	—	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	—	—	0.5	Bit periods

8.4 PCM Timing

The BCM43013 supports two independent PCM interfaces that share the pins with the I2S interfaces. The PCM Interface on the BCM43013 can connect to linear PCM Codec devices in master or slave mode. In master mode,the BCM43013 generates the PCM_CLK and PCM_SYNC signals; in slave mode, these signals are provided by another master on the PCM interface and are inputs to the BCM43013. The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Short Frame Sync, Master Modem

PCM Timing Diagram (Short Frame Sync, Master Mode)

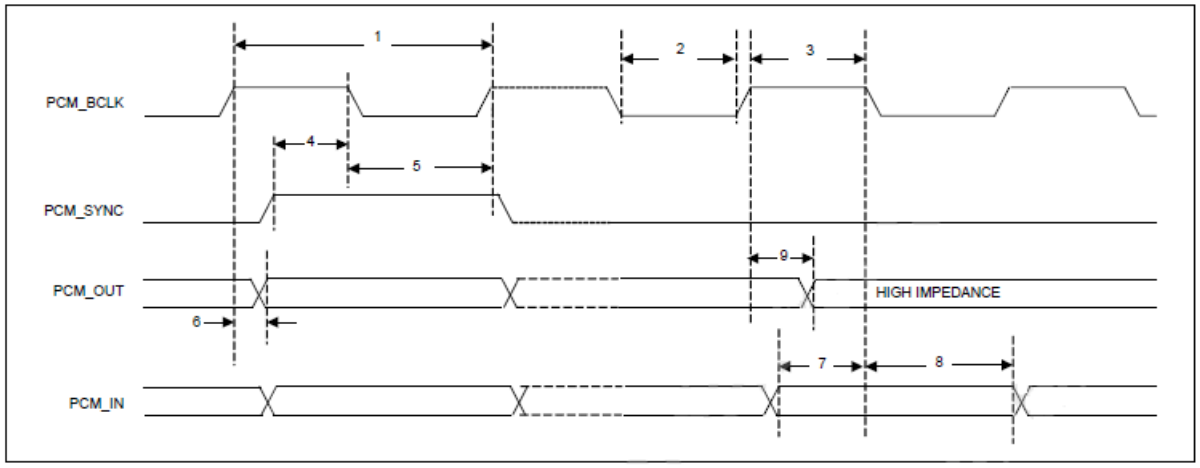


PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Slave Mode

PCM Timing Diagram (Short Frame Sync, Slave Mode)

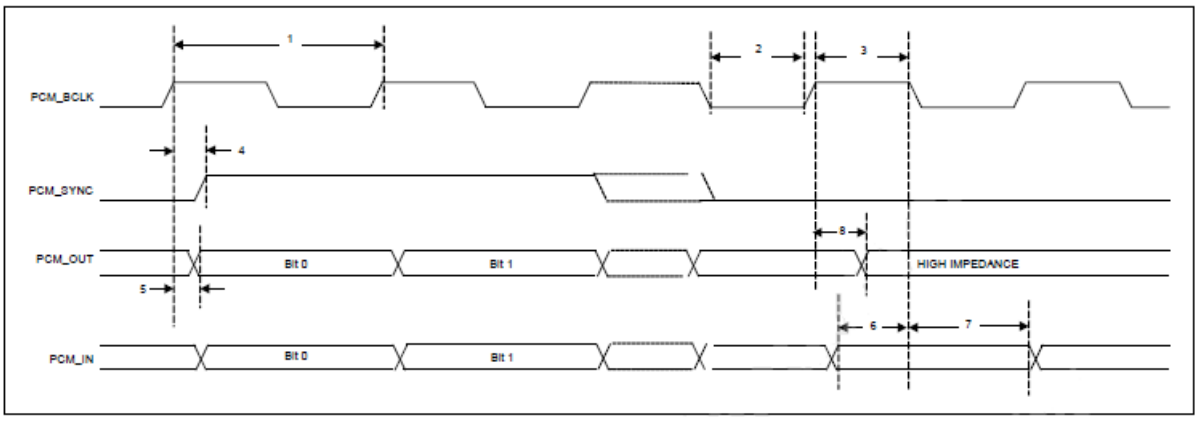


PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Master Mode

PCM Timing Diagram (Long Frame Sync, Master Mode)

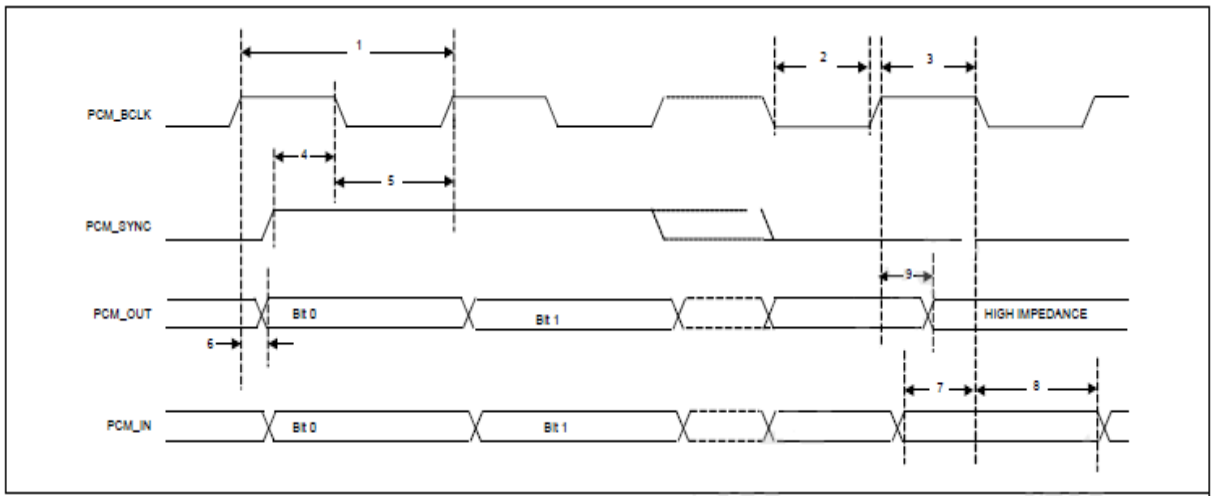


PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Slave Mode

PCM Timing Diagram (Long Frame Sync, Slave Mode)

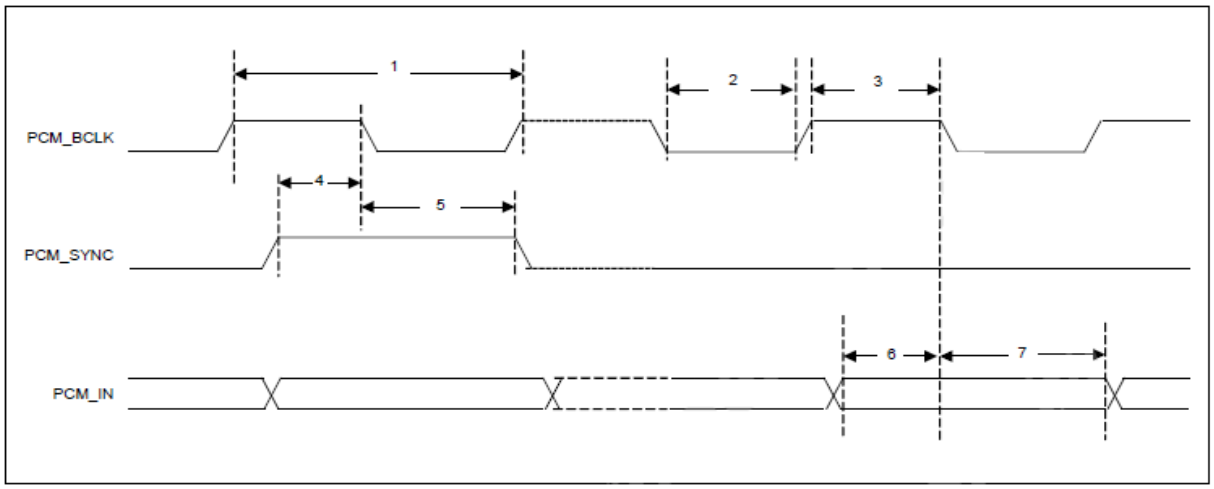


PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Short Frame Sync)

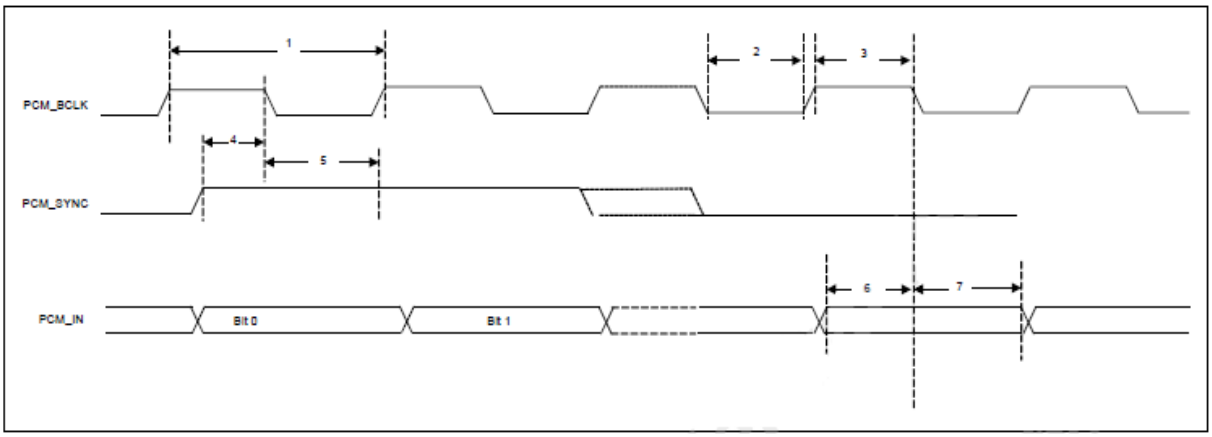


PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

Long Frame Sync, Burst Mode

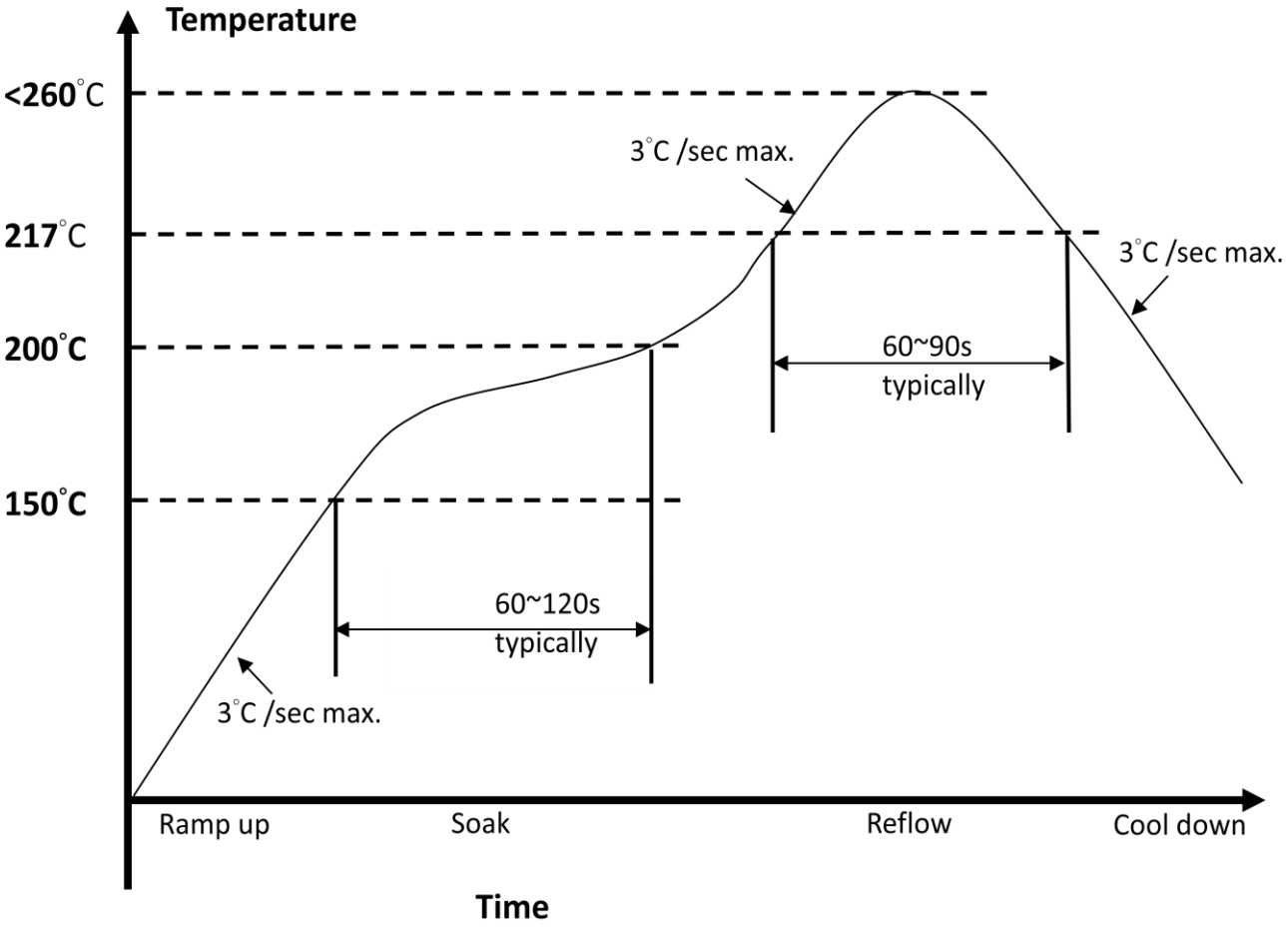
PCM Burst Mode Timing (Receive Only, Long Frame Sync)



PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

9. Recommended Reflow Profile



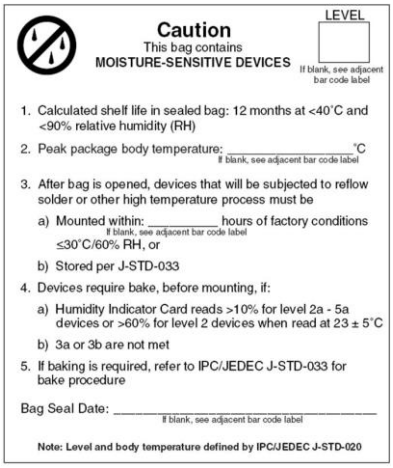
1. Referred to IPC/JEDEC standard
2. Peak Temperature : <260°C
3. Cycle of Reflow : 2 times max.
4. Adding Nitrogen (N2) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
5. If the shelf time is exceeded, be sure baking step to remove the moisture from the component

10. Package Information

10.1 Label

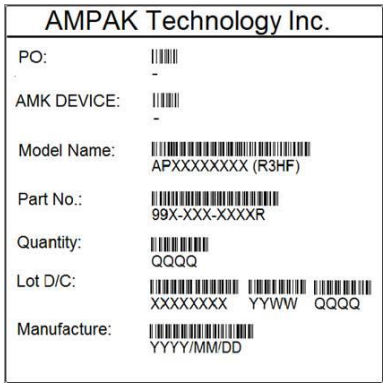
Label A→ Anti-static and humidity notice

Label B→ MSL caution / Storage Condition

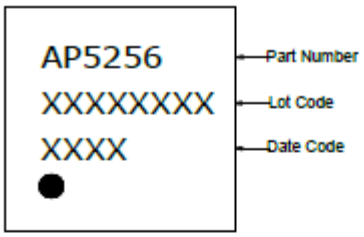


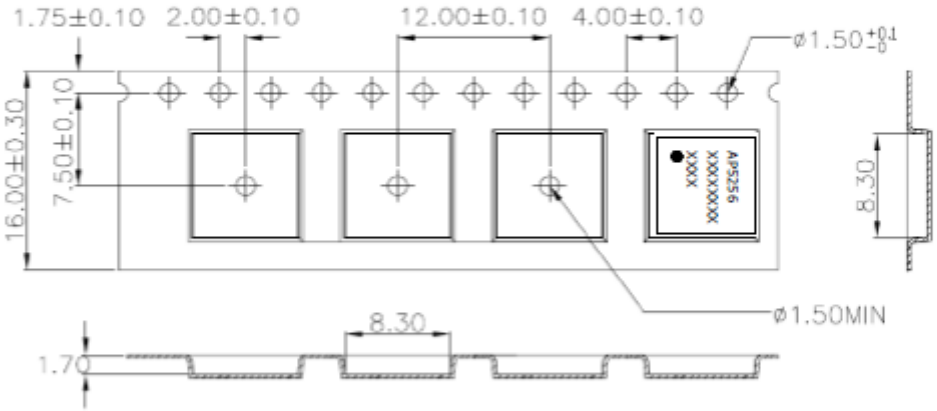
Label C→ Inner box label .

Label D→ Carton box label .



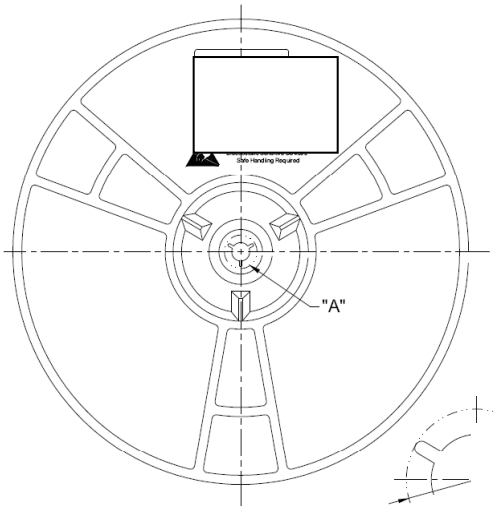
10.2 Dimension

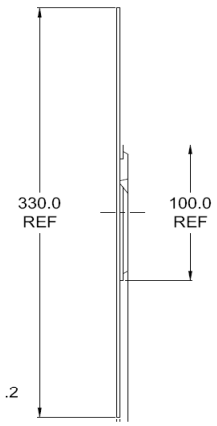


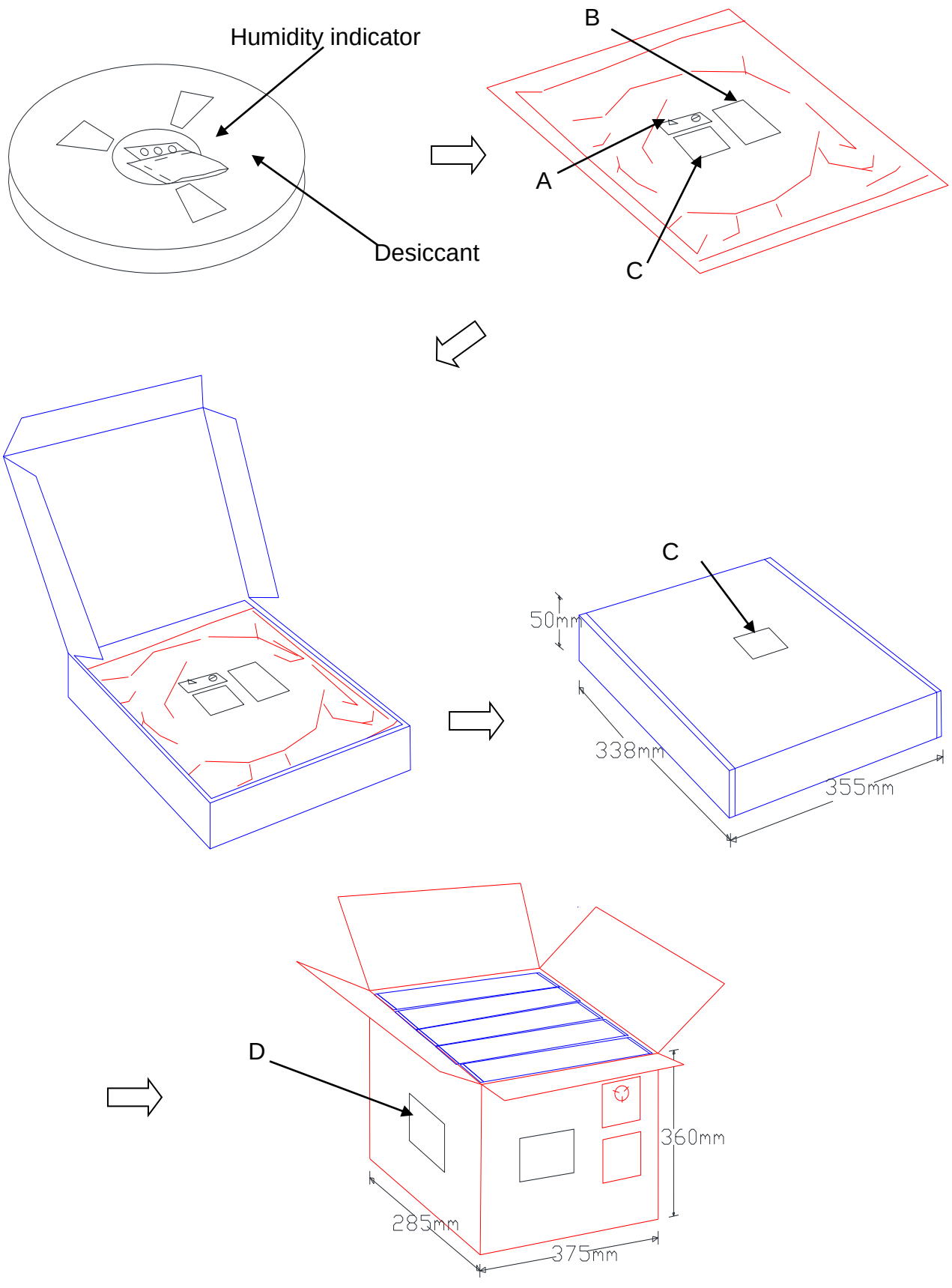


1. 10 sprocket hole pitch cumulative tolerance ±0.20.
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy.
4. All dimensions meet EIA-481-D requirements.
5. Thickness : 0.30±0.05mm.
6. Component load per 13" reel : 1500 pcs

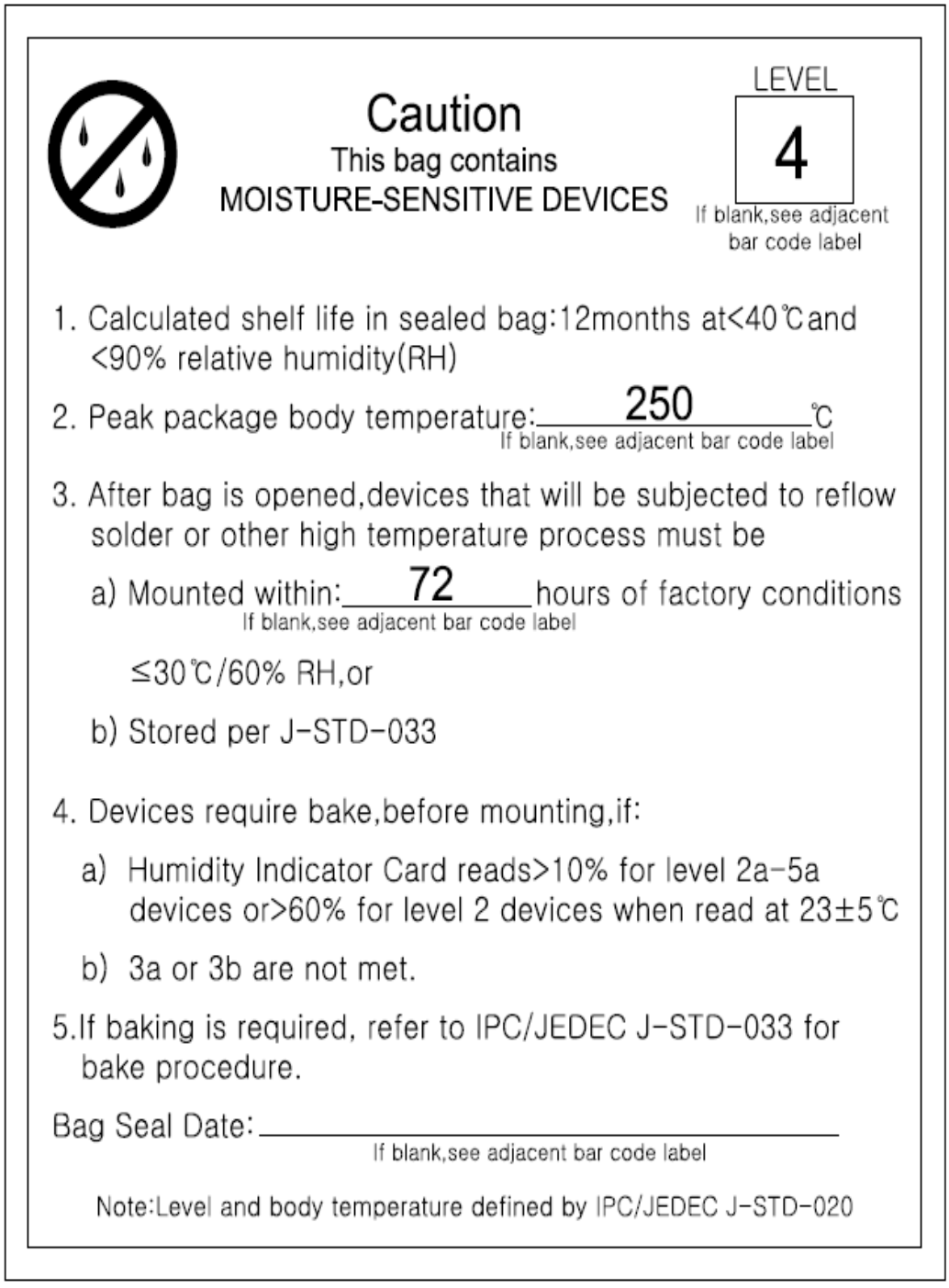
W	16.00±0.30
A0	8.30±0.10
B0	8.30±0.10
K0	1.70±0.10






Humidity indicator
Desiccant
B
A
C
C
50mm
338mm
355mm
D
360mm
285mm
375mm

10.3 MSL Level / Storage Condition



Caution

This bag contains
MOISTURE-SENSITIVE DEVICES

LEVEL 4

If blank,see adjacent bar code label

1. Calculated shelf life in sealed bag:12months at<40℃and <90% relative humidity(RH)
2. Peak package body temperature:___250___℃
   If blank,see adjacent bar code label
3. After bag is opened,devices that will be subjected to reflow solder or other high temperature process must be
   a) Mounted within:___72___hours of factory conditions
      If blank,see adjacent bar code label
      ≤30℃/60% RH,or
   b) Stored per J-STD-033
4. Devices require bake,before mounting,if:
   a) Humidity Indicator Card reads>10% for level 2a-5a devices or>60% for level 2 devices when read at 23±5℃
   b) 3a or 3b are not met.
5. If baking is required, refer to IPC/JEDEC J-STD-033 for bake procedure.

Bag Seal Date:_____
If blank,see adjacent bar code label

Note:Level and body temperature defined by IPC/JEDEC J-STD-020